FERROELECTRICS - APPLICATIONS

Edited by **Mickaël Lallart**

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Preface

Ferroelectricity has been one of the most used and studied phenomena in both scientific and industrial communities. Properties of ferroelectrics materials make them particularly suitable for a wide range of applications, ranging from sensors and actuators to optical or memory devices. Since the discovery of ferroelectricity in Rochelle Salt (which used to be used since 1665) in 1921 by J. Valasek, numerous applications using such an effect have been developed. First employed in large majority in sonars in the middle of the 20th century, ferroelectric materials have been able to be adapted to more and more systems in our daily life (ultrasound or thermal imaging, accelerometers, gyroscopes, filters…), and promising breakthrough applications are still under development (non-volatile memory, optical devices…), making ferroelectrics one of tomorrow's most important materials.

The purpose of this collection is to present an up-to-date view of ferroelectricity and its applications, and is divided into four books:

- *Material Aspects*, describing ways to select and process materials to make them ferroelectric.
- *Physical Effects*, aiming at explaining the underlying mechanisms in ferroelectric materials and effects that arise from their particular properties.
- *Characterization and Modeling*, giving an overview of how to quantify the mechanisms of ferroelectric materials (both in microscopic and macroscopic approaches) and to predict their performance.
- *Applications*, showing breakthrough use of ferroelectrics.

Authors of each chapter have been selected according to their scientific work and their contributions to the community, ensuring high-quality contents.

The present volume focuses on the applications of ferroelectric materials, describing innovative systems that use ferroelectricity. The current use of such devices as sensors and actuators, in the field of acoustics, MEMS, micromotors and energy harvesting will be presented in chapters 1 to 5. The next section proposes a particular emphasis

on the application of ferroelectric materials as transistors and memory devices (chapters 6 to 11), showing one of the future breakthrough uses of these materials.

I sincerely hope you will find this book as enjoyable to read as it was to edit, and that it will help your research and/or give new ideas in the wide field of ferroelectric materials.

Finally, I would like to take the opportunity of writing this preface to thank all the authors for their high quality contributions, as well as the InTech publishing team (and especially the publishing process manager Ms. Silvia Vlase) for their outstanding support.

June 2011

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Part 1

Sensors and Actuators

1

Giant k_{31} Relaxor Single-Crystal Plate and Their Applications

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1. Introduction

Typical ferroelectric ceramics, lead zirconate titanate (PZT) ceramics are widely used for devices of electrical-mechanical energy conversion devices such as sensors and actuators, which correspond to the five senses and foot & hand of human being. Recently, these devices spread out in the computer controlled fields, for example, robotics and mechatronics. The research and development of ferroelectric ceramics, particularly PZT ceramics, have mainly focused on the material compositions to realize new electronic devices utilizing their piezoelectric properties. Many researchers in companies and institutes have carried out R & D on such chemical compositions since the discovery of piezoelectricity in PZT ceramics by Jaffe et al. in 1954. On the other hand, through the new research on DC poling field dependence of ferroelectric properties in PZT ceramics, the poling field has become an effective tool for evaluation and control of the domain structures, which fix the dielectric and ferroelectric properties of PZT ceramics. Therefore, PZT ceramics with different domain structures can be fabricated even though the ceramic compositions remain the same. These ceramics are called poling field domain controlled ceramic. It is thought that the domain controlled ceramics will lead to a breakthrough and the appearance of new ferroelectric properties. The study on the clarification of relationships between [compositions] vs [poling fields] vs [dielectric and piezoelectric properties] in hard and soft PZT ceramics was applied to other ferroelectric materials of lead titanate ceramics, lead-free ceramics such as barium titanate, alkali bismuth niobate, alkali bismuth titanate ceramics and relaxor single crystals of $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ (PZNT91/09) and $Pb[(Mg_{1/3}Nb_{2/3})_{0.74}Ti_{0.26}]O_3$ (PMNT74/26) compositions.
This chapter describes how can be achieved the new ferroelectric properties such as giant transverse-mode electromecanical coupling factor of k_{31} over 80% and piezoelectric strain d_{31} constant of -2000 pC/N in PZNT91/09 and PMNT74/26 single crystals realized a mono-domain single crystal by accurately controlling the domain structures. In addition, high-efficiency piezoelectric unimorph and bimorph are also discribed as the devices using giant k_{31} single crystals.

2. Giant electromechanical coupling factor of k_{31} mode and piezoelectric d_{31} constant in $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ single-crystal plates

Ferroelectric single crystals made of compounds such as $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ (PZNT91/09) have been attracting considerable attention, because of the large longitudinal-

mode electromechanical coupling factor of k_{33} over 92%. Since high-quality and large crystals are necessary to develop devices such as transducers for medical use, we have undertaken and succeeded in the fabrication of PZNT91/09 single crystals with large dimensions. In addition, for further applications to sensors and actuators, a large k_{31} (d_{31}) mode as well as a large k_{33} (d_{33}) mode are needed.

2.1 Single-crystal sample preparation

The single crystals evaluated were grown by a solution Bridgman method with a Pt crucible supported at the bottom by a conical insulator stand. The crystals without Pt contamination from the crucible have the dimensions of 50 mm (2 inches) diameter, 35 mm height, and 325 g weight. The as-grown single crystals were cut along [100] of the original cubic direction confirmed by X-ray diffraction and from Laue photographs. The single-crystal samples with dimensions of 4.0^{W}(width)x13^{L}(length)x0.36^{T}(thickness) mm for k_{31}, k_t and d_{31} and 4.2^{W}x4.2^{L}x12^{T} mm for k_{33} and d_{33} were prepared to evaluate the dielectric and piezoelectric properties. Gold electrodes for the following DC poling and electrical measurements were fabricated by conventional sputtering. Poling was conducted at 40 ^{o}C for 10 min by applying 1.0 kV/mm to obtain resonators with various vibration modes.

2.1.1 What is "giant k_{31} piezoelectricity"?

Figure 1 shows the frequency responses of the impedance in k_{33} and k_{31} modes in the cases of various coupling factors. It is easy to explain the wide frequency band, which corresponds to the difference between anti-resonant frequency (fa) and resonant frequency (fr), in higher coupling factors. An early work on a PZNT91/09 single crystal poled

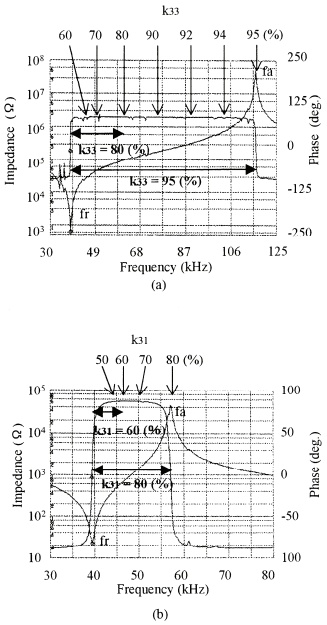


Fig. 1. Frequency and phase responses of (a) k_{33} and (b) k_{31} fundamental modes in the cases of various coupling factors.

along [001] of the original cubic direction found that the values of k_{31} (d_{31}) and k_{33} (d_{33}) modes were 62% (-493 pC/N) and 92% (1570 pC/N), respectively. In a more recent work, the k_{31} (d_{31}) mode of 53% (-1100 pC/N) and the k_{33} (d_{33}) mode of 94% (2300 pC/N) were reported for $Pb[(Zn_{1/3}Nb_{2/3})_{0.92}Ti_{0.08}]O_3$ (PZNT92/08) single crystals poled along [001]. There are significant differences in the k_{31} and d_{31} modes between our result and the previous results, despite finding almost the same k_{33} (95%) and d_{33} (2500pC/N).
A large difference between k_{31}=80.8% and $-d_{31}$=1700 pC/N in this study and k_{31}=53-62% and $-d_{31}$=493-1100 pC/N in the previous studies for the single crystals is considered to be due to the following. It is well known that dielectric and piezoelectric properties are strongly affected by the quality of the crystals. It was pointed out that a small portion of opaque parts in the crystal wafer significantly reduces the electromechanical coupling factor of the crystals. Since PZNT91/09 crystals evaluated in this study have very high transparency with a minimum defect level thus far reported, due to better control of the Bridgman crystal growth, the highest k_{31} and d_{31} can be obtained.

2.1.2 Where does "giant k_{31} piezoelectricity" come from?

Figures 2(a) and 2(b) show the temperature dependences of k_{31}, k_{33} and elastic compliance (s_{11}^E). Higher k_{31} and k_{33} were obtained in the rhombohedral phase below 80 °C. The values of s_{11}^E in the rhombohedral phase are larger than those in the tetragonal phase. Furthermore, the frequency constant (fc=frxL, where L is length), which corresponds to half the bulk wave velocity, of the k_{31} mode (fc_{31} =522 Hz·m) is relatively small in comparison with that of lead zirconate titanate (PZT) ceramics (fc_{31}=1676 Hz·m). We believe that the high piezoelectricity in the PZNT91/09 single crystal is due to the mechanical softness of the rhombohedral phase, not the existence of a MPB, for easy deformation by the poling field. This concept may be supported by the result that high k_{33} (>90%) independent of the rhombohedral composition, such as PZNT91/09, PZNT92/08 or $Pb[(Zn_{1/3}Nb_{2/3})_{0.955}Ti_{0.045}]O_3$ (PZNT95.5/4.5), was obtained.

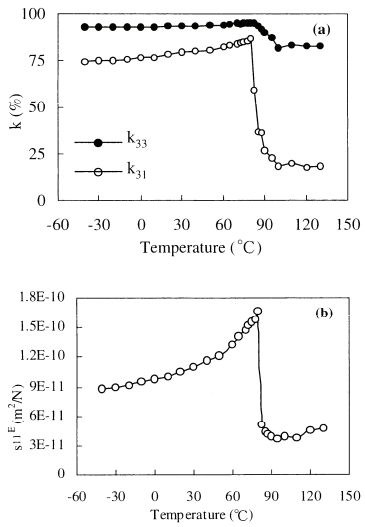


Fig. 2. Temperature dependences of (a) electromechanical coupling factors (k_{31} and k_{33}) and (b) elastic compliance (s^E_{11}) in PZNT91/09 single crystal.

In conclusion of this part, frequency spectrum analysis of the responses to vibration modes was carried out in detail utilizing large PZNT91/09 single crystals of high quality. Giant k_{31} and d_{31}, as well as k_{33} and d_{33}, were obtained by efficient and uniform DC poling, it means a mono-domain structure in the single-crystal plate as described the next part. The crystals with these giant k_{31} and d_{31} will be applied for use in sensors and actuators with high performance.

2.2 Origin of giant piezoelectricity in PZNT91/09 single-crystal plates

In order to clarify the origin of giant piezoelectricity in PZNT91/09 single-crystal plates, the poling field dependence of dielectric and ferroelectric properties were investigated in single-crystal samples with demension of $4.0^{W}x13^{L}x0.36^{T}$ mm for k_{31}, k_t and d_{31} and $4.2^{W}x4.2^{L}x12^{T}$ mm for k_{33} and d_{33}. The poling field dependence was carried out as follows; the poling was conducted at 40 °C for 10 min while varying the poling field (E) from 0 to 2000 V/mm. After each poling, the dielectric and piezoelectric properties were measured at room temperature using an LCR meter, an impedance analyzer and a d_{33} meter. Moreover, the domain structures were observed under polarized light with crossed nicols by an optical microscope.

2.2.1 DC poling field dependence of dielectric constant, d_{33} constant, k_{31}, k_t, k_{33} and their frequency constants of fc_{31} and fc_t

Figure 3 shows the effect of DC poling field (E) on dielectric constant ($\varepsilon_{33}^{T}/\varepsilon_0$) and piezoelectric d_{31} and d_{33} constants. There were three stages in $\varepsilon_{33}^{T}/\varepsilon_0$ with increasing E. The first stage was E<400 V/mm, the second stage was 400 V/mm≦E<1000 V/mm, and the third stage was E≧1000 V/mm. These stages in terms of dielectric constant mean that there are three thresholds of domain rotation and switching in the direction of the poling field. From our previous study, E of 300 V/mm in the first stage corresponds to the coercive field (Ec) and E of 180° domain clamping on PZNT91/09 single crystals. While d_{33} has approximately the same tendency as the dielectric constant for the poling field, d_{31} decreased abruptly over 1500 V/mm in the third stage. The giant $-d_{31}$ of nearly 1700 pC/N could be obtained at 1000 V/mm≦E<1500 V/mm. On the other hand, the highest d_{33} of nearly 2500 pC/N could be obtained at 1000 V/mm≦E≦2000 V/mm. It was thought that the difference between d_{31} and d_{33} at 1500 V/mm≦E≦2000 V/mm was due to the difference in the domain structure in the directions of the length and the thickness for the sample plate ($4.0^{W}x13^{L}x0.36^{T}$ mm).

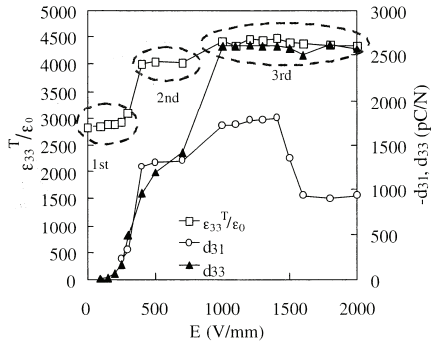


Fig. 3. Poling field dependence of dielectric constant, and piezoelectric d_{31} and d_{33} constants (poling temperature: 40 °C, time: 10 min).

Figure 4 shows the effect of poling field (E) on the electromechanical coupling factors (k_{31}, k_{33}) and frequency constant (fc_{31}). The plots of the poling field vs k_{33} and k_{31} were almost the same as the plots of the poling field vs d_{33} and d_{31} shown in Fig. 3. While the giant k_{31} of over 80% was obtained at 1000 V/mm≦E<1500 V/mm, the highest k_{33} of over 90% was obtained at 1000 V/mm≦E≦2000 V/mm. Furthermore, the frequency constant of the k_{31} mode (fc_{31}) showed the lowest value of nearly 500 Hz·m at 1000 V/mm≦E<1500 V/mm. Therefore, it was found that the giant k_{31} (d_{31}) and the minimum fc_{31} appeared simultaneously at the specific poling fields of 1000 V/mm≦E<1500 V/mm. With increasing E from 1500 V/mm to 2000 V/mm, k_{31} decreased and fc_{31} increased abruptly without any change in k_{33}. The behavior observed for the poling field vs k_{31} (d_{31}) and fc_{31} in the third region suggested that a mono-domain in the length direction (the direction perpendicular to the poling field) was achieved at 1000 V/mm≦E<1500 V/mm, and further, the mono-domain changed into a number of domains (multi-domains in the plate) in the length direction at 1500 V/mm≦E≦2000 V/mm.

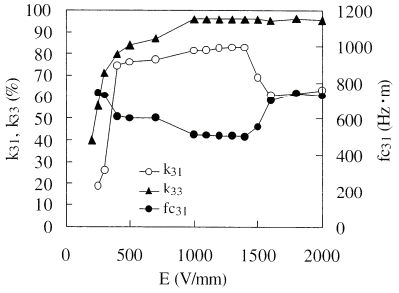


Fig. 4. Poling field dependence of k_{31} and k_{33}, and frequency constant fc_{31} (poling temperature: 40°C, time: 10 min).

Figure 5 shows the effect of poling field (E) on electromechanical coupling factor (k_t) and frequency constant (fc_t). The k_t mode and fc_t correspond to the thickness vibration for the sample plate ($4.0^W x 13^L x 0.36^T$ mm). While k_{33} increased from 80% to 95% with increasing E from 400 V/mm to 2000 V/mm in Fig. 4, k_t and fc_t were independent of the poling field in the same range of E. We believe the difference in the poling field dependence between k_{33} and k_t is due to the effect of the domain structure on the vibrations of k_{33} and k_t modes in the thickness direction for the sample plate.

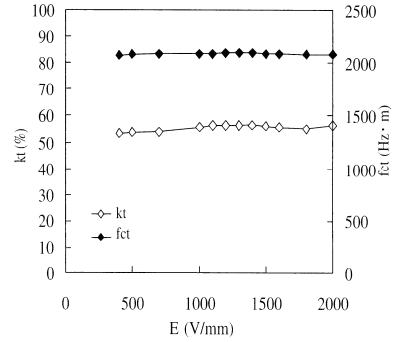


Fig. 5. Poling field dependence of k_t and frequency constant fc_t (poling temperature: 40 °C, time: 10 min).

2.2.2 Domain structures of single-crystal plates at various poling fields

After each poling at E, both the surfaces of the sample plate ($4.0^{W}x13^{L}x0.36^{T}$ mm) were polished and the domain structure in the plate area ($4.0^{W}x13^{L}$ mm) was observed under polarized transmission light with crossed nicols. The frequency responses of the impedance in k_{31} mode were also measured at every poling field. Figures 6(a)~6(d) show the domain structures and the frequency responses in k_{31} mode. The as-grown crystal mainly had black and brown stripes as shown in Fig. 6(a). We believe that the stripes consist of 180° domains alongside their domain walls. By applying E of 350 V/mm for 10 min at 40 °C, the brown area increased, the boundaries between black and brown stripes became unclear and the single response of the k_{31} (47%) mode was obtained [Fig. 6(b)]. A mono-domain crystal without domain walls was confirmed to exist at E=1000 V/mm. In addition, the giant k_{31} of nearly 80% appeared in the mono-domain crystal with the single response and with the minimum frequency constant of fc_{31} mode [Fig. 6(c)]. The

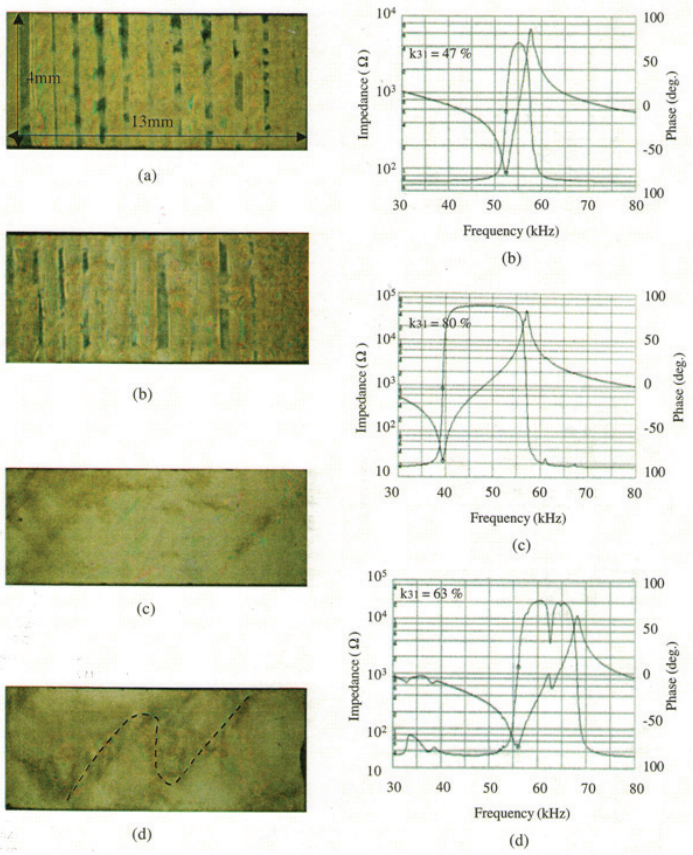


Fig. 6. Poling field dependence of domain structures in sample plate area ($4.0^{W}x13^{L}$ mm) and frequency responses of impedance and phase on k_{31} mode; (a) as-grown (before poling), (b) E=350 V/mm, (c) E=1000 V/mm and (d) E=2000 V/mm; the thickness of the plate is 0.36 mm and the broken line in Fig. 6(d) indicates a domain boundary.

frequency constant (fc_{31}) corresponds to half the bulk wave velocity (v_{31}), and further, there is a relationship between the Young's modulus (Y) of the crystal and fc_{31} as follows:

$$v_{31} = 2 \times fc_{31} = 2 \times fr \times L = Y^{1/2} \bullet \rho^{-1/2},$$

where fr and ρ are the resonant frequency of k_{31} mode and the bulk density of the crystal, respectively. Therefore, it is said that the most softened (i.e., with the lowest v_{31} or fc_{31}) PZN91/PT09 crystals poled by the specific poling conditions (1000 V/mm≦E<1500 V/mm at 40 °C for 10 min) are essential to achieve the giant k_{31} and d_{31}. With E greater than 1500 V/mm, since the mono-domain changed into the muluti-domains, the single response of the k_{31} mode was divided into two responses and the value of fr or fc_{31} increased. As a consequence, k_{31} was reduced to 63% [Fig. 6(d)]. It was thought that the reason only a few domains were formed was the generation of strain in the direction perpendicular to the poling field - namely, not in the sample thickness of 0.36^{T} mm but in the sample plate area of $4.0^{W}x13^{L}$ mm, in the crystal poled by the higher poling field. This is summarized schematically in Fig. 7 for the relationships among the poling fields and the domain structures. In addition, Table 1 shows the relationships among the Young's modulus (Y), k_{33} and k_{31} for various materials. It is found that the Y ($0.89x10^{10}$ N/m^2) in rhombohedral PZNT91/09 with giant k_{31} is one order of magnitude smaller than the Y ($6\sim9x10^{10}$ N/m^2) of PZT ceramics and, roughly speaking, one order of magnitude larger than the Y ($0.05x10^{10}$ N/m^2) of rubber. Therefore, we believe that the giant k_{31} of over 80% arises from the remarkable softness of the domain controlled single crystal due to the poling field.

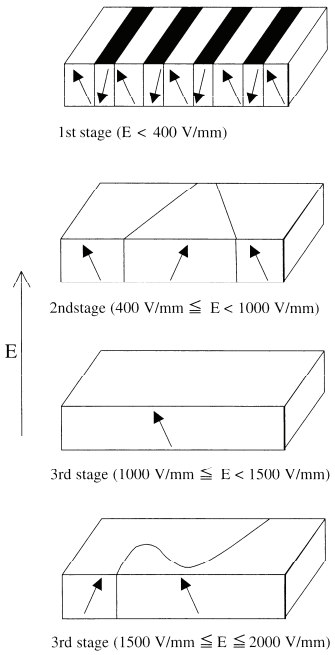


Fig. 7. Schematics of domain structures (↖↙↖↙↖) in PZNT91/09 single crystal under various poling fields; the arrow of E shows the direction of the poling field.

Material	Y ($\times 10^{10}$ N/m^2)	k_{33} (%)	k_{31} (%)
PZNT 91/09	0.89* (2.58)**	95	80
Soft PZT ceramics	6	70	40
Hard PZT ceramics	9	60	30
$PbTiO_3$ ceramics	13	50	6
$BaTiO_3$ ceramics	11	45	15
Steel	20	—	—
Rubber	0.05	—	—

*Rhombohedral phase, **Tetragonal phase.

Table 1. Relationships among Young's modulus (Y), k_{33} and k_{31} in various materials.

In conclusion of this part, the origin of PZNT91/09 single crystals with giant k_{31} of over 80% and $-d_{31}$ constant nearly 1700 pC/N were due to a mono-domain structure in the crystal plates. Controlling the poling conditions, the crystal plate with multi-domains changed into one having the mono-domain in the direction perpendicular to the poling field as well as in the direction parallel to the poling field. Futhermore, this ferroelectric domain controlled single crystal by a poling field possessed the lowest frequency constant of fc_{31}.

3. Giant k_{31} in $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ single-crystal plates

Another relaxor single crystal of $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMNT) is investigated in detail regarding the k_{31} mode and the conditions for obtaining giant k_{31} and d_{31} constant are clarified.

3.1 Crystal plane dependence of giant k_{31} in $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ single-crystal plates

Recently, a giant k_{31} over 86% and a piezoelectric d_{31} constant of nearly -2100 pC/N were found for a (100) $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ (PZNT91/09) single crystal poled in the [001] direction. In order to realize giant k_{31}, it was the significant relationship between the crystal plane and the poling direction. Moreover, it was clarified that the giant k_{31} and d_{31} constant could be obtained with a poling temperature of 40 °C in the rhombohedral phase and with sufficient poling fields of 1000~1500 V/mm. The origin of the giant k_{31} and d_{31} constant was found to be due to the mono-domain structure in the direction perpendicular to the poling field as well as in the direction parallel to the poling field. In this part, we investigate the relationships between the crystal planes and the poling direction in $(1-x)Pb(Mg_{1/3}Nb_{2/3})O_3$-$xPbTiO_3$ [PMNT(1-x)/x] single-crystal plates to obtain giant k_{31}.

3.1.1 Realization of giant k_{31} in PMNT plates

Figure 8 shows the DC poling field (E) dependence of relative dielectric constant (ε_r) and k_{31} in (100) PMNT68/32 and (110) PMNT74/26 single-crystal plates. The ε_r (■) in (100) PMNT has a peak at E=300 V/mm and decreases with increasing E. There is aging in ε_r (■) and k_{31} (□) for (100) PMNT, after 16 and 64 h at room temperature. The same phenomena were observed in (110) PZNT91/09 single-crystal plates poled in the [110] direction. On the other hand, the ε_r (●) and k_{31} (○) in (110) PMNT increased abruptly at E=200 V/mm and reached constant values without aging. It was found that a giant k_{31} of over 86% was obtained at $E \geqq 200$ V/mm in (110) PMNT single-crystal plates at the poling temperature of 40 °C.

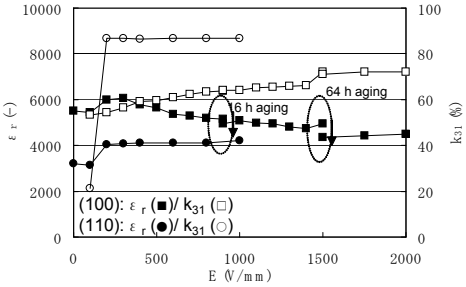


Fig. 8. DC poling field dependence of ε_r and k_{31} in (100) and (110) PMNT single-crystal plates.

The effects of poling temperature on k_{31}, d_{31} constant and the frequency constant (half of the bulk wave velocity) of the k_{31} mode (fc_{31}) in (110) PMNT74/26 single-crystal plates are shown in Fig. 9. The temperatures of 40 ºC (○), 100 ºC (□) and 120 ºC (Δ) correspond to the pseudo-cubic phase, the phase boundary between pseudo-cubic and tetragonal phases, and the tetragonal phase, respectively (Fig. 10). It is confirmed that giant k_{31} and d_{31} constant were obtained to polarize (110) PMNT plates in pseudo-cubic phase (the poling temperature of 40 ºC), while applying $E \geqq 200$ V/mm. In addition, the giant k_{31} and d_{31} constant were accompanied by the lowest fc_{31}, nearly 700 Hz·m. These results were the same as those of (100) PZNT91/09 single-crystal plates with giant k_{31}.

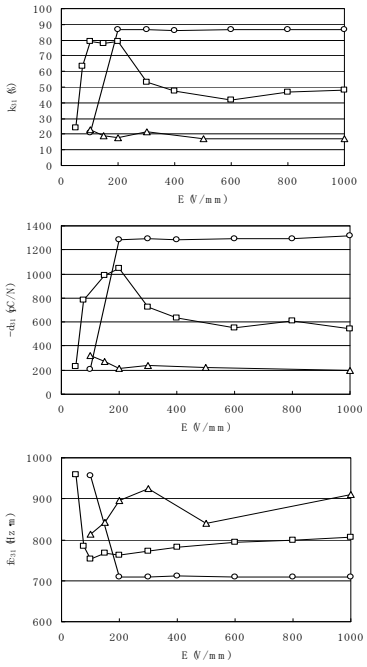


Fig. 9. DC poling field dependence of k_{31}, d_{31} and fc_{31} in (110) PMNT74/26 single-crystal plates at poling temperatures of 40 ºC (○), 100 ºC (□) and 120 ºC (△).

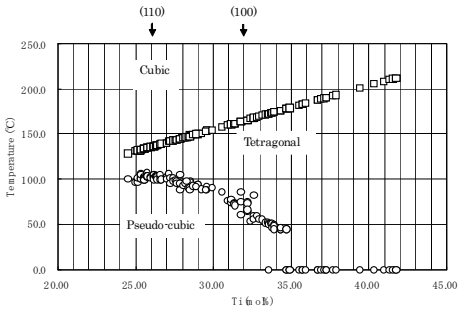


Fig. 10. Phase diagram of $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ single crystals grown by a solution Bridgman method.

3.1.2 Impedance response analysis of giant k_{31}

Figures 11(a), (b) and Figs. 12 (a), (b) show the frequency responses of impedance on the fundamental k_{31} modes and up to 500 kHz in the cases of (100) and (110) PMNT single-crystal plates poled at 40 °C, E=1000 V/mm and 10 min. The values of k_{31} in (100) and (110) PMNT single-crystal plates were 42.6% and 84.6% (giant k_{31}), respectively. The k_{31} fundamental and its overtones were observed to have complicated spurious responses in (100) PMNT in Fig. 12(a). However, the k_{31} fundamental and its 3rd, 5th, 7th and 9th overtones were confirmed not to have spurious responses in (110) PMNT with giant k_{31} in Fig. 12(b), and were also confirmed the frequency responses of impedance in (100) PZNT91/09 single-crystal plates with giant k_{31}. Therefore, it is found that a single vibration was generated in the direction of the length (L). In order to clarify the resonance response near 300 kHz [inside the ellipse in Fig. 12(b)], the original single-crystal plate (13^Lx4.0^Wx0.47^T mm) was cut to the small plate dimensions (0.97^Lx4.0^Wx0.47^T mm). The k_{32} in

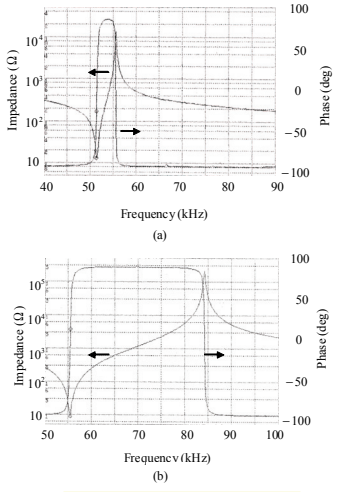


Fig. 11. Impedance and phase responses of the fundamental k_{31} mode in (a) (100) and (b) (110) PMNT single-crystal plates.

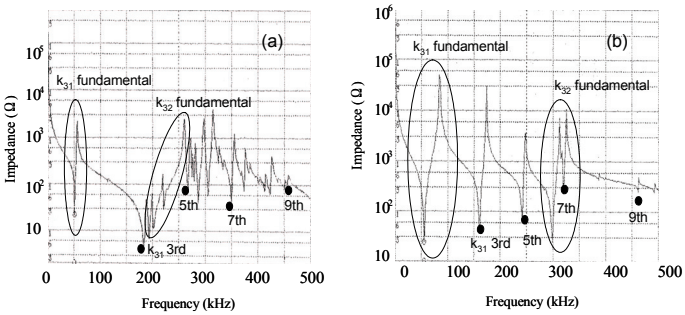


Fig. 12. Frequency responses of impedance in fully poled (a) (100) and (b) (110) PMNT single-crystal plates (DC poling conditions: 40 °C, 1000 V/mm, 10 min).

the width (W) direction was 69%, which was calculated from the resonance response of the small plate. Furthermore, the frequency constants on the k_{31} (length direction) and k_{32} (width direction) modes became 680 Hz·m and 1425 Hz·m, respectively. Consequently, it was found that the (110) PMNT single-crystal plate with giant k_{31} possessed an anisotropy in the frequency constant on the 13^{L}x4.0^{W} mm plate and consisted of a mono-domain as in the case of the (100) PZNT91/09 single-crystal plate with giant k_{31}.

3.1.3 Relationship between crystal plane and poling direction

The mechanism for realizing giant k_{31} can be explained by using the crystal plane and poling direction. Figure 13 shows the relationship between the crystal plane, which determines the direction of the spontaneous polarization, and the poling direction in (100) and (110) PMNT single-crystal plates. While applying the poling field to the (100) PMNT single-crystal plate at a poling temperature of 40 °C (pseudo-cubic phase), the poling field only acts to expand the x-axis in the direction of the poling field. In the (110) PMNT plate, the poling field acts to generate strain via the expansion of the x and y-axes (Fig. 13), which moves the ferroelectric domains on the (110) plane. While the domain structure on the (110) plane became singular due to the generated strain, it is thought that the anisotropy of the frequency constants on the k_{31} and k_{32} modes appeared and the giant value of the k_{31} mode in (110) PMNT was achieved through the poling process.

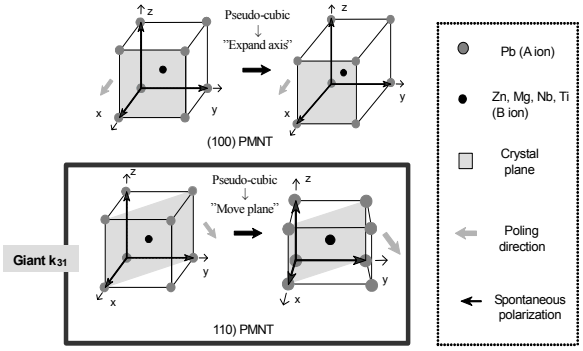


Fig. 13. Relationship between crystal plane, direction of the spontaneous polarization and poling direction in (100) and (110) PMNT single-crystal plates at 40 °C (pseudo-cubic phase).

Table 2 shows the values of k_{31}, k_{32}, d_{31} and d_{33} constants in PMNT and PZNT single-crystal plates with various crystal planes. Although giant k_{31} and d_{31} constant were obtained in the (110) PMNT plate, a large d_{33} constant (2420 pC/N) was realized in the (100) PMNT plate. On the other hand, giant k_{31}, d_{31} constant, and large d_{33} constant (2400 pC/N) were obtained simultaneously in the (100) PZNT91/09 plate. Therefore, it was clarified that giant k_{31}, d_{31} and d_{33} constants appeared in the peculiar combination of the crystal plane and poling direction in the relaxor single crystals. Moreover, there was anisotropy on the k_{31} (length direction) and k_{32} (width direction) modes in (110) PMNT with giant k_{31} as well as in (100) PZNT with giant k_{31}.

Crystal plane	Single crystal	k_{31} (%)	$-d_{31}$ (pC/N)	k_t (%)	d_{33} (pC/N)	k_{32} (%)	Pr ($\mu C/cm^2$)	Ec (V/mm)	Aging
(100)	PZNT	86	2100	55	2400	42	35	600	Good
(100)	PMNT	65	1030	60	2420		22	300	NG
(110)	PZNT	30~60	300~720	40	530~1030				NG
(110)	PMNT	87	1320	48	970	69	30	200	Good
(111)	PZNT	20	~170	50	190~560				Good

Table 2. Giant k_{31} and d_{31} constant in PMNT and PZNT single-crystal plates with various crystal planes. k_t is the coupling factor of thickness vibration in a plate, and piezoelectric d_{33} constant was measured with a d_{33} meter.

In conclusion of this part, giant k_{31} over 86% in (110) PMNT single-crystal plates was realized in order to control the relationship between the crystal plane, which determines the direction of the spontaneous polarization, and the poling direction. The plate with giant k_{31} shows the impedance responses with a single vibration generated in the length direction. It is thought that the origin of giant k_{31} is the mono-domain structure in the plate.

3.2 Chemical composition dependnce of ginat k_{31} in PMNT single-crystal plates

A giant electromechanical coupling factor of k_{31} mode of more than 86% was found for (100) $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ (PZNT91/09) single-crystal plates ($13^L x 4.0^W x 0.36^T$ mm) and (110) $Pb[(Mg_{1/3}Nb_{2/3})_{0.74}Ti_{0.26}]O_3$ (PMNT74/26) single-crystal plates ($13^L x 4.0^W x 0.47^T$ mm) poled in the [001] and [110] directions, respectively. In this part, the chemical composition dependence of k_{31} mode in PMNT single-crystal plates with (110) plane is investigated in detail and furthermore, the relationships between the crystal phase after poling and giant k_{31} are clarified.

3.2.1 Ti composition dependence of ginat k_{31}

The (110) PMNT(1-x)/x (x=0.251~0.301) single-crystal plates in this study have pseudo-cubic phase before poling below 100 °C (x=0.25) and 90 °C (x=0.30). Figure 14 shows the relationships between relative dielectric constant (ε_r) before and after poling [Fig. 14(a)], k_{31} and the frequency constant (half the bulk wave velocity) of k_{31} mode (fc_{31}) [Fig. 14(b)], and the electromechanical coupling factor of the thickness vibration mode of the plate (k_t) and frequency constant of k_t mode (fc_t) [Fig. 14(c)] versus Ti composition (x) in (110) PMNT(1-x)/x single-crystal plates. Although ε_r (○) in (110) PMNT is almost constant and abruptly increases for x>0.293 before poling, ε_r (●) after poling is divided into four groups 1~4: group 1 (x=0.251~0.255), group 2 (x=0.269~0.279), group 3 (x=0.291~0.293) and group 4

(x=0.296~0.301) in Fig. 14(a). Since the groups of ε_r correspond to the groups of the domain structure, it was thought that the PMNT single-crystal plates processed different domain structures in each group after DC poling. On the other hand, k_{31} increases with an increase in x and reaches a maximum of 92% at x=0.291. After that, k_{31} suddenly decreases with x as shown in Fig. 14(b). The fc_{31} also has four groups and shows an opposite tendency compared with k_{31} vs x. This means that higher k_{31} is obtained for lower fc_{31}, because the decrease in the number of domain boundaries through the improvement of the poling process in the single-crystal plates leads to a decrease in stiffness. Since k_t and fc_t are independent of x in Fig. 14(c), the domain structures are almost the same in the thickness direction of the plates. Therefore, the chemical composition dependence of ε_r after poling, k_{31} and fc_{31} appears to be dependent on the domain structure in the plate (13^{L}x4.0^{W} mm).

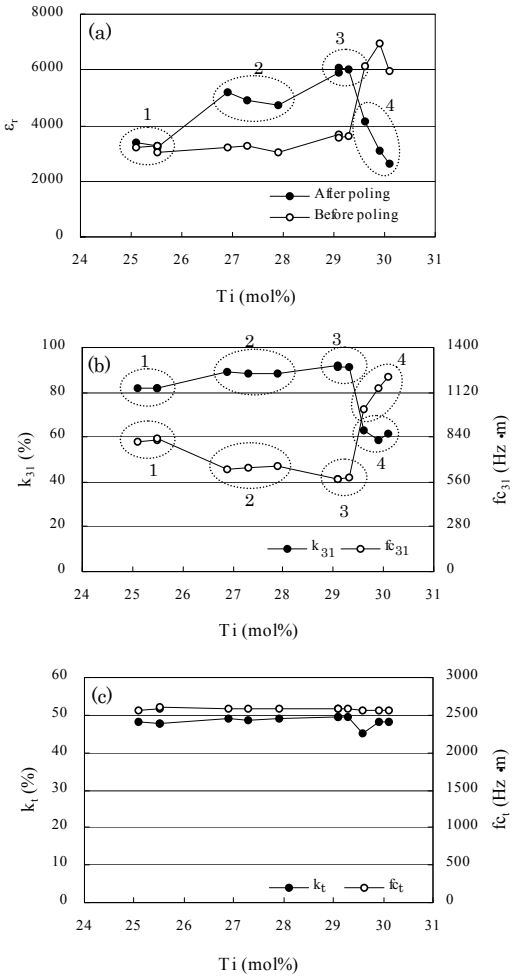


Fig. 14. Ti composition dependence of (a) ε_r before and after poling, (b) k_{31}, fc_{31} and (c) k_t, fc_t in PMNT(1-x)/x single-crystal plates.

3.2.2 Impedance response analysis of ginat k_{31}

Figure 15 shows the frequency responses of impedance to 500 kHz in the cases of groups 1~4 in Fig. 14. The k_{31} fundamental and their odd-number overtones of 3rd, 5th, 7th and 9th with the k_{32} fundamental vibration (width direction) were confirmed without spurious responses in groups 1~3 in (110) PMNT with giant k_{31}, as well as the frequency response of impedance in the (100) PZNT91/09 single-crystal plate with giant k_{31}. However, the k_{31} fundamental and their overtones were observed with complicated spurious responses in group 4 in the (110) PMNT with k_{31}=60%. Therefore, it was found that a single vibration is generated in the direction of the length (L) in the (110) PMNT with giant k_{31}, similar to the case of the (100) PZNT91/09 single-crystal plate with giant k_{31}.

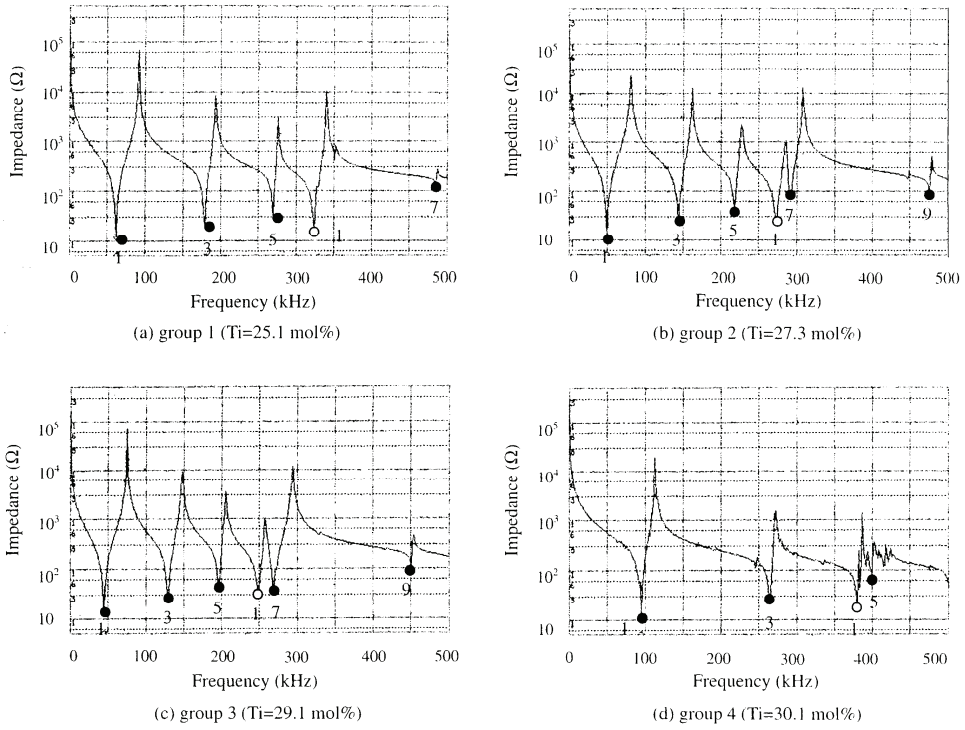


Fig. 15. Frequency responses of impedance in fully poled (110) PMNT(1-x)/x single-crystal in cases of (a) group 1, (b) group 2, (c) group 3 and (d) group 4 (●1: k_{31} fundamental vibration, ●3-9: k_{31} odd-number overtones, ○1: k_{32} fundamental vibration; DC poling conditions: 40°C, 1000 V/mm, 10 min).

3.2.3 Crystal phase to realize ginat k_{31}

A mechanism to realize giant k_{31} can be explained by the crystal plane, which strongly affects the direction of the spontaneous polarization and poling direction. Giant k_{31} in relaxor single-crystal plates can be achieved when the poling field generates sufficient strain to move the ferroelectric domains in the plates (13^{L}x4.0^{W} mm), not merely to expand the spontaneous polarization axes in the direction of the poling field. We will

discuss in detail the relationships between crystal planes, spontaneous polarization axes and poling direction in (110) PMNT single-crystal plates (groups 1~4) in comparison with the cases of (100) and (110) PZNT91/09 single-crystal plates (see Fig. 27 in the paragraph 4.2.3). Furthermore, it will be clarfied that the crystal phases after poling can be estimated by the value of k_{31} and the combination between the directions of the spontaneous polarization axes and the poling field, which generates the strain sufficient to move the domains in the plates.
In conclusion of this part, giant k_{31} of more than 80% in (110) PMNT single-crystal plates was clarified to possess Ti composition dependence. The frequency response of impedance in (110) PMNT single-crystal plates with giant k_{31} was composed of a single vibration in the length direction. In addition, the domain movement to realize giant k_{31} in the crystal plate was due to the combination between the direction of the spontaneous polarization and the poling direction.

4. Other characteristics investigation

The giant k_{31} and d_{31} constant in the PZNT91/09 and PMNT(1-x)/x single-crystal plates were due to the generation of a single vibration in the length direction. However, there is as yet no evidence of the close relationship between the mono-domain plate with a giant k_{31}, which means a single vibration body, and the single vibration in the plates measured from the impedance response.
Furthermore, the P-E hysteresis loops and the relationship to electric field (E) vs strain measurement were investigated from the viewpoints of giant k_{31}.

4.1 Frequency response analysis by finite element method in relaxor single-crystal plates with ginat k_{31}

In this part, the frequency response analysis of impedance on the giant k_{31} mode is evaluated by a finite element method (FEM) in order to characterize the mono-domain plates. Since the number of ferroelectric domains in the plates corresponds to the number of piezoelectric vibration bodies, the frequency response analysis by FEM was applied to the evaluation of their domain structures. Moreover, the domain behavior of the PZNT91/09 single-crystal plates is also investigated by FEM, particularly focusing on the 3rd overtone of the k_{31} fundamental vibration.

4.1.1 FEM application

Resonators composed of relaxor single-crystal plates, the dimensions of which are 13^{L}x4.0^{W}x0.36^{T} mm, with a giant k_{31} in PZNT91/09 with the (100) plane and PMNT74/26 with the (110) plane were analyzed using a commercial analysis program (ANSYS) by FEM. For the FEM simulation, an electric field of 1.0 V/mm to simulate the impedance responses was added in the thickness direction of the plate resonators because the actual voltage to be measured was 0.5 V by the impedance analyzer. The material constants obtained from the measured and reference data on the relaxor single crystals were used to calculate the impedance responses. The numbers of the elements and nodes for FEM were 800 pieces and 4271 points, respectively. Piezoelectric equations were applied to the orthorhombic phase. Furthermore, Poisson ratio in the length direction (k_{31} mode) and width direction (k_{32} mode)

was measured from the impedance responses by single-crystal plate resonators with different dimensions. In order to evaluate domain structures in the single-crystal plates, the relationships between the number of domains in the PZNT91/09 single-crystal plates and the 3rd overtone splitting of the k_{31} fundamental vibration were also investigated by FEM simulation.

Table 3 shows the coupling factors of k_{31}, k_{32} and their frequency constants (fr x L or W, where fr is the resonant frequency) of fc_{31}, fc_{32} in the relaxor single-crystal plates with a giant k_{31} of more than 80%. The values of σ_W^E/σ_L^E in Table 3 were calculated from the elastic compliance of s_{11}^E and s_{22}^E because $\sigma_L^E=-(s_{12}^E/s_{11}^E)$ and $\sigma_W^E=-(s_{12}^E/s_{22}^E)$, where σ_L^E and σ_W^E are the Poisson ratios in the directions of length (13 mm) and width (4 mm), respectively. In the simulation, σ_W^E/σ_L^E was used to evaluate the crystal anisotropy of the relaxor single crystals, because of the difficulty in measuring the values of s_{12} in the single crystals. It was confirmed that there are large crystal anisotropies of s_{11}^E and s_{22}^E between the L and W directions and large differences in σ_W^E/σ_L^E of 3.4 (PZNT91/09) and 4.5 (PMNT74/26), respectively.

single crystal	k_{31} (%)	k_{32} (%)	fc_{31} (Hz·m)	fc_{32} (Hz·m)	s_{11}^E (10^{-12} m²/N)	s_{22}^E (10^{-12} m²/N)	σ_W^E/σ_L^E
PZNT91/09	86	42	520	830	110	32	3.4
PMNT74/26	87	69	683	1425	67	15	4.5

Table 3. Material constants of relaxor single-crystal plates with giant k_{31}.

Although the values of k_t (coupling factor of plate thickness vibration) and fc_t (frequency constant of the k_t mode) of the PZNT91/09 and PMNT74/26 single-crystal plates with a giant k_{31} were 57, 49% and 2087, 2588 Hz·m, respectively, it was thought the crystal structure of the plate resonators after DC poling becomes a field-induced phase such as the orthorhombic phase, because of the anisotropy of the bulk wave velocities (twofold the frequency constant) in the length (L=13 mm), width (W=4.0 mm) and thickness (T=0.36 mm) directions. Furthermore, a giant k_{31} could be obtained only in the orthorhombic phase after DC poling from the relationships between the directions of the spontaneous polarization and DC poling field to move domains in the plate (13^Lx 4.0^W mm).

4.1.2 Simulation of k_{31} and k_{32} modes by FEM

The change in the values of σ_W^E and σ_L^E affected the frequency response of impedance on k_{31} fundamental vibration, the overtones, and k_{32} fundamental vibration in the frequency range of 0~500 kHz. The simulated response at $\sigma_W^E/\sigma_L^E=3.2$ ($\sigma_L^E=0.089$, $\sigma_W^E=0.29$) and $s_{12}^E=-10$ (10^{-12} m²/N) was well fitted to the measured responses, as shown by the arrows in Fig. 16, in the case of the PZNT91/09 single-crystal plate. The simulated data at $\sigma_W^E/\sigma_L^E=4.9$ ($\sigma_L^E=0.041$, $\sigma_W^E=0.20$) and $s_{12}^E=-3$ (10^{-12} m²/N) in the PMNT74/26 single-crystal plates also showed the same result (Fig. 17). In the calculations, the values of s_{12}^E were chosen to fit the simulated responses to the measured responses. Moreover, the Poisson ratio affected the value of k_{31} as well as the frequency response of impedance.

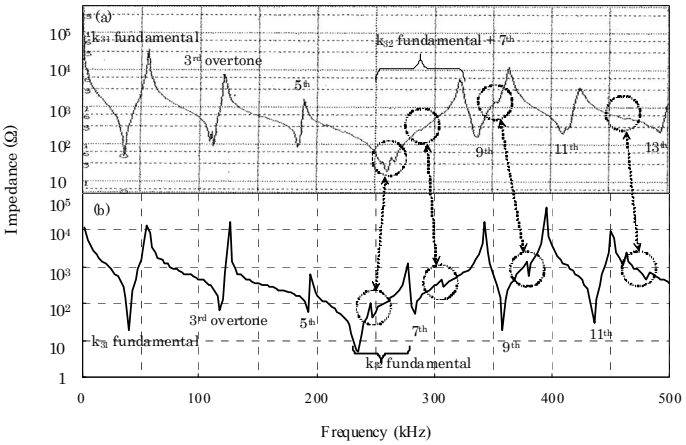


Fig. 16. Frequency responses of impedance on k_{31} and k_{32} modes in PZNT91/09 single-crystal plates; (a) measured and (b) simulated data.

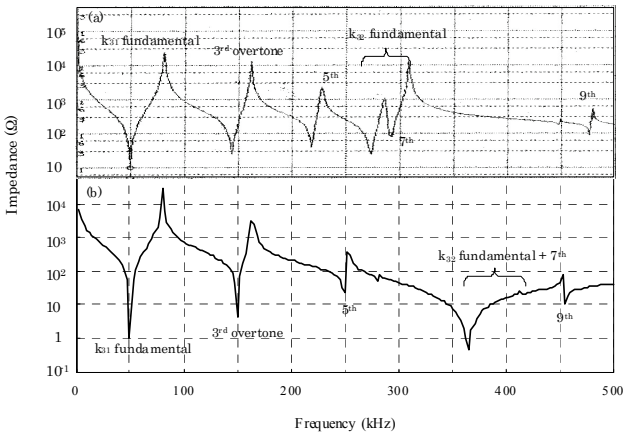


Fig. 17. Frequency responses of impedance on k_{31} and k_{32} modes in PMNT74/26 single-crystal plates; (a) measured and (b) simulated data.

4.1.3 Simulation of k_t mode by FEM

The impedance responses up to 30 MHz in Fig. 18 were calculated in the PZNT91/09 single-crystal plates at σ_W^E/σ_L^E=3.2, σ_L^E=0.045-0.13, and σ_W^E=0.15-0.41. The k_t fundamental vibration and the 3rd and 5th overtones of the k_t fundamental vibration were observed between σ_L^E=0.063-0.11 and σ_W^E=0.20-0.35. In particular, sharp responses of the k_t fundamental vibration and the 3rd overtone were obtained between σ_L^E=0.080-0.098 and σ_W^E=0.26-0.32. The simulated coupling factor of k_t=64% was higher than that of k_t=57% calculated from the measured response. It was clarified that the large difference in σ_W^E/σ_L^E=3.2 and the suitable values of the elastic compliance, particularly $-s_{12}^E$=9-11 (10^{-12} m²/N), were key factors for the appearance of the k_t fundamental vibration and overtones.

The simulated response of the PMNT74/26 single-crystal plates is shown in Fig. 19 at σ_W^E/σ_L^E=4.9 (σ_L^E=0.041, σ_W^E=0.20) and s_{12}^E=-3 (10^{-12} m²/N). The fundamental k_t mode (k_t=65%) and the 3rd overtone were observed independent of $-s_{12}^E$ values between 1~7 (10^{-12} m²/N). In the calculations, the values of $-s_{12}^E$ were chosen at a Poisson ratio (σ_W^E) within 0~0.5.

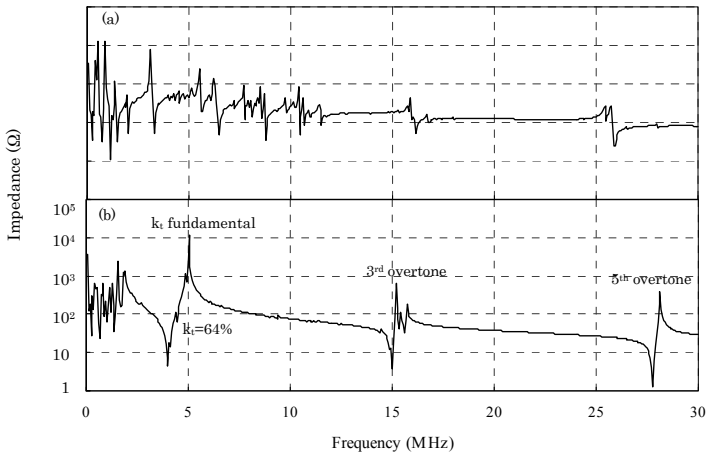


Fig. 18. Frequency responses of impedance on k_t mode in PZNT91/09 single-crystal plates; calculation for (a) σ_W^E/σ_L^E=3.2 (σ_L^E=0.13, σ_W^E =0.41)/ s_{12}^E=-14 (10^{-12} m²/N) and (b) σ_W^E/σ_L^E=3.2 (σ_L^E=0.089, σ_W^E =0.29)/ s_{12}^E=-10 (10^{-12} m²/N).

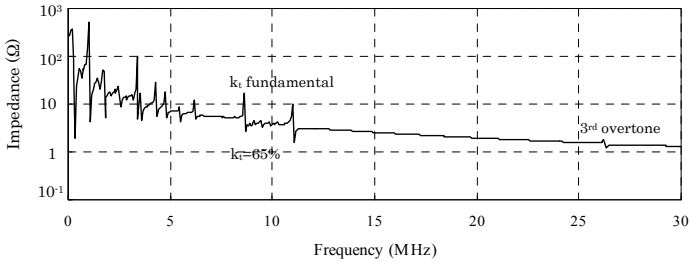


Fig. 19. Frequency responses of impedance on k_t mode in PMNT74/26 single-crystal plates; calculation for σ_W^E/σ_L^E=4.9 (σ_L^E=0.041, σ_W^E =0.20) and s_{12}^E=-3 (10^{-12} m²/N).

Figure 20 shows the impedance and phase responses of k_t fundamental vibration in the PZNT91/09 single-crystal plates. The impedance response consisted of four peaks split into ①-④ in the cases of the simulated and the measured responses. Herein, the PZNT91/09 plate resonator with a giant k_{31} of 84% was prepared under the poling conditions of a DC poling field (E) of 1200 V/mm. Although the simulation for the splitting was calculated from the values of σ_W^E/σ_L^E=3.2 (σ_L^E=0.089, σ_W^E=0.29) and s_{12}^E=-10 (10^{-12} m²/N), the splitting of the four peaks occurred in the case of a giant k_{31} in the PZNT91/09 single-crystal plates. Therefore, it was confirmed that the simulation data were exactly fitted to the measured data in both the

cases of the generation of the k_t mode and the impedance and phase responses of the k_t fundamental vibration. The impedance and phase responses of the k_t fundamental vibration of PMNT74/26 single-crystal plates are shown in Fig. 21 [$\sigma_W{}^E/\sigma_L{}^E$=4.9 ($\sigma_L{}^E$=0.041, $\sigma_W{}^E$=0.20) and $s_{12}{}^E$=-3 (10^{-12} m²/N)] in comparison with the measured responses. The simulated impedance and phase responses were well fitted to the measured responses.

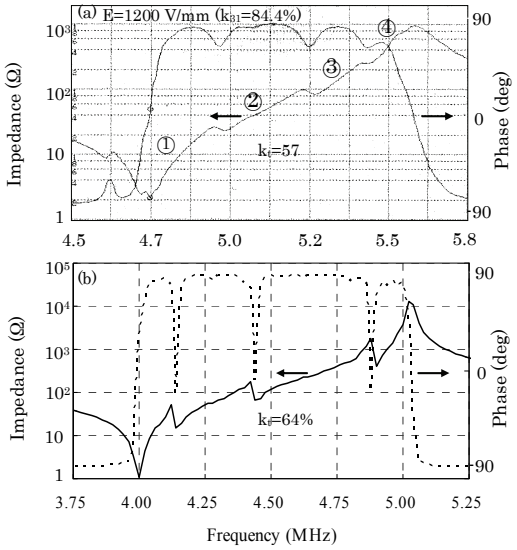


Fig. 20. Frequency responses of impedance and phase on k_t fundamental vibration in PZNT91/09 single-crystal plates; (a) measured and (b) simulated data.

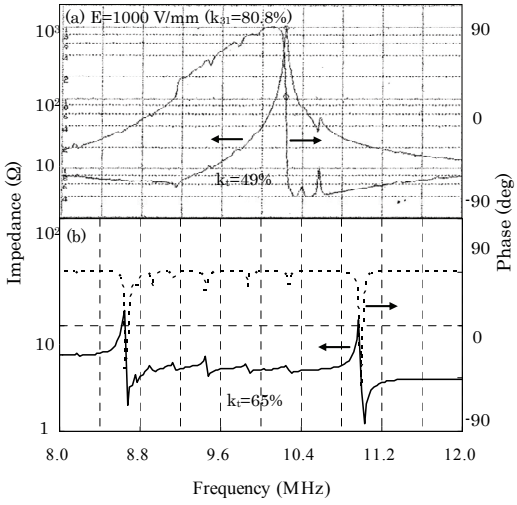


Fig. 21. Frequency responses of impedance and phase on k_t fundamental vibration in PMNT74/26 single-crystal plates; (a) measured and (b) simulated data.

4.1.4 Domain behavior evaluation by FEM

The 3rd overtone in the k_{31} mode was calculated to synthesize one-third of the simulated responses each in the cases of (i) $\sigma_W{}^E/\sigma_L{}^E$=2.5 ($\sigma_L{}^E$=0.13, $\sigma_W{}^E$=0.32), (ii) $\sigma_W{}^E/\sigma_L{}^E$=2.4 ($\sigma_L{}^E$=0.13, $\sigma_W{}^E$=0.31), and (iii) $\sigma_W{}^E/\sigma_L{}^E$=1.8 ($\sigma_L{}^E$=0.17, $\sigma_W{}^E$=0.31). The simulated 3rd overtone response consisted of three peaks splitting in PZNT91/09 [shown in the circle of Fig. 22(a)]. On the other hand, the plate resonator DC poled at E=400 V/mm, the poling field of which is just below that required to obtain a giant k_{31}, also possesses the 3rd overtone with three peaks splitting [shown in the circle of Fig. 22(b)]. Therefore, it was thought that the PZNT91/09 single-crystal plate was composed of three vibration bodies, namely, three large domains with $\sigma_W{}^E/\sigma_L{}^E$ values of 2.5, 2.4, and 1.8. Since the splitting of the three peaks of the 3rd overtone response formed one peak at E= 1200 V/mm obtaining a giant k_{31} of 84.4% (shown in the circle of Fig. 22(c)), it was proved that a mono-domain plate with a giant k_{31} was achieved. From our study, it was confirmed that frequency response analysis of impedance is an effective tool for the evaluation of domain structures in single-crystal plates.

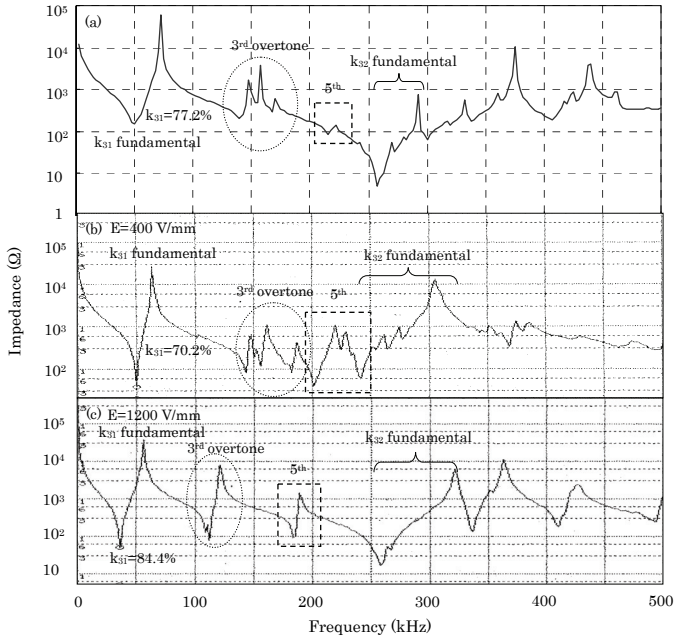


Fig. 22. Frequency responses of impedance on 3rd overtone on k_{31} mode in PZNT91/09 single-crystal plates; (a) simulated data, (b) measured data of plate resonator DC poled at E=400 V/mm, and (c) measured data of plate resonator DC poled at E=1200 V/mm.

4.1.5 Origin of giant k_{31} from viewpoints of material constants

The most significant factors for realizing giant piezoelectricity in the k_{31} mode in the relaxor single-crystal plates were thought as follows: Firstly, large $s_{11}{}^E$ values of 110 (10^{-12} m^2/N) in the PZNT91/09 single-crystal plates and 67 (10^{-12} m^2/N) in the PMNT74/26 single-crystal plates in the direction of length were required (Table 3). These $s_{11}{}^E$ values are relatively

larger than that of 11-17 (10^{-12} m^2/N) in PZT ceramics. This means that the single-crystal plates with a giant k_{31} of more than 80% became markedly soft and showed a low Poisson ratio, particularly σ_L^E<0.1 after DC poling. Secondly, a large anisotropy of bulk wave velocity (twofold the frequency constant) accompanied by a large σ_W^E/σ_L^E=3.2-3.4 in PZNT91/09 single-crystal plates and a large σ_W^E/σ_L^E=4.5-4.9 in PMNT74/26 single-crystal plates was essential. Therefore, it was thought that the physical meaning of the above-mentioned large s_{11}^E, low σ_L^E, and large σ_W^E/σ_L^E originated from a field-induced phase such as the orthorhombic phase by DC poling because the combination of the directions of spontaneous polarization and poling field in the orthorhombic phase could only move domains in the plates.

In conclusion of this part, impedance response analysis by FEM was performed using the k_{31}, k_{32}, and k_t modes in relaxor single-crystal plates with a giant k_{31}. It was found that a large anisotropy on the k_{31} and k_{32} modes was generated in the plate resonators with a giant k_{31}. As the Poisson ratios of the length and width directions in the plates were changed, the simulation results were well fitted to the measured impedance responses. These results could be explained by the material constants in a field-induced phase induced by the DC poling field. Furthermore, the domain behavior in the single-crystal plates was evaluated from the synthesized impedance response of three vibration bodies, i.e., three domains with different Poisson ratios.

4.2 Giant k_{31} and d_{31} in relaxor single-crystal plates evaluated using P-E hysteresis loops and strain

The longitudinal-mode electromechanical coupling factor k_{33} of over 90% was easy to obtain because the vibration direction of the k_{33} mode is the same as that of the poling field. However, the relationship between the giant k_{31} and k_{33} modes is not clarified. In this part, we could explain the relationship using P-E hysteresis loops and electric field (E) vs strain measurement from the viewpoint of giant k_{31}.

4.2.1 P-E hysteresis loops

Figure 23 shows the electric field (E) dependence of P-E hysteresis loops in (100) PZNT91/09 single-crystal plate measured at 40℃ by a high voltage test system. While a symmetrical P-E loop was observed at E = 1000 V/mm, a triple loop was generated as E ≧ 1500 V/mm in the case of the crystal plate with giant k_{31}.

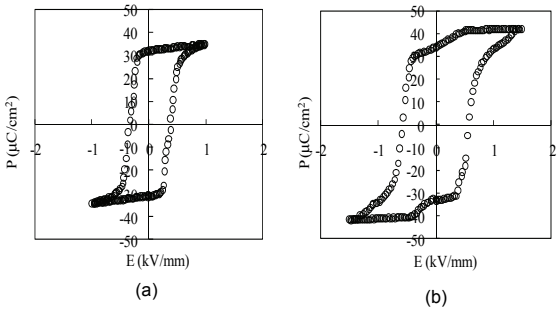
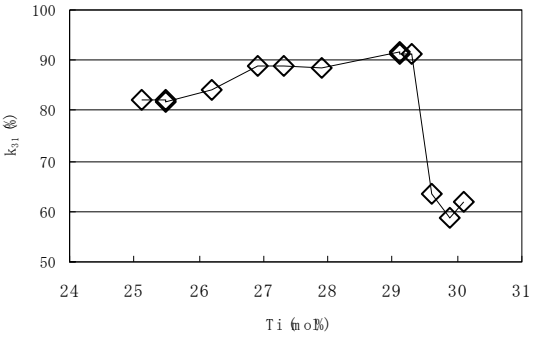


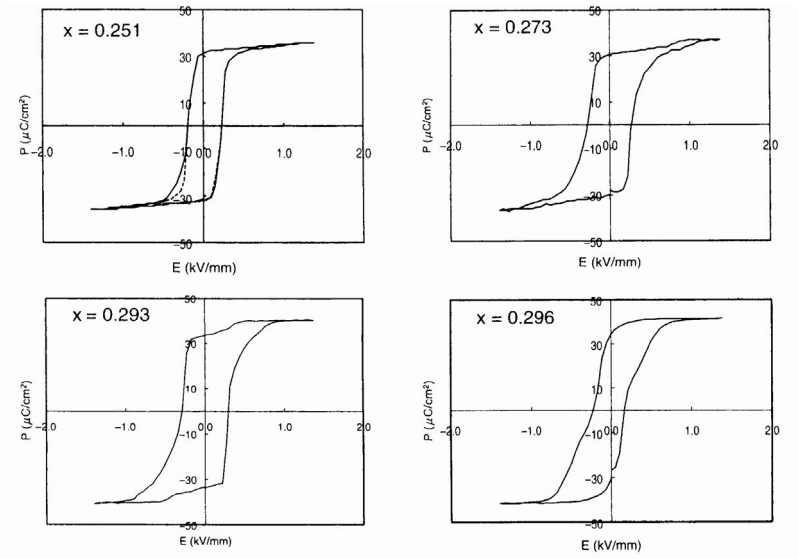
Fig. 23. P-E hysteresis loops in PZNT91/09 single-crystal plates (a) before (E=1000 V/mm) and (b) after (E=1500 V/mm) the appearance of giant k_{31} over 80%.

Therefore, it was considered that the E of 1500 V/mm is a coercive field to obtain giant k_{31}. In addition, the triple loops were realized at 20-60 °C, in the rhombohedral phase of PZNT91/09.

Figure 24 shows the Ti composition (x) dependence of k_{31} [Fig. 24(a)] and P-E loops [Fig. 24(b)] in PMNT(1-x)/x single-crystal plate measured at 40 °C (pseudo-cubic phase) under E =1500 V/mm. Although a symmetrical P-E hysteresis loop was obtained at x = 0.296-0.301 in the plate with k_{31}=60%, triple loops were observed at x=0.273-0.293, and asymmetrical loops were observed at x=0.251-0.262 in the plates with giant k_{31} (>80%). The E=800 V/mm to generate the triple and asymmetrical loops corresponds to a coercive field to realize giant k_{31}.



(a)



(b)

Fig. 24. Ti composition (x) vs (a) k_{31} and (b) P-E hysteresis loops in PMNT(1-x)/x single-crystal plates; x=0.251 (asymmetrical part near dotted lines), x=0.273/ 0.293 (triple loop at high E), and x=0.296 (symmetrical loop).

4.2.2 Shrinkage strain characteristics

Figure 25 shows the dependence of the shrinkage strain measured at room temperature (rhombohedral phase of PZNT91/09) on the electric field (E) applied in the same direction as the DC poling field using a photonic sensor. A large hysteresis regarding E vs strain appeared between 400 and 1500 V/mm, the E of which (1500 V/mm) is the coercive field to obtain giant k_{31} in PZNT91/09. The large hysteresis for E vs shrinkage strain corresponds to the large hysteresis for E vs expansion strain in PZNT91/09 single crystal. Therefore, it was found that the large hysteresis for E vs strain (shrinkage and expansion) is due to the generation of giant k_{31}.

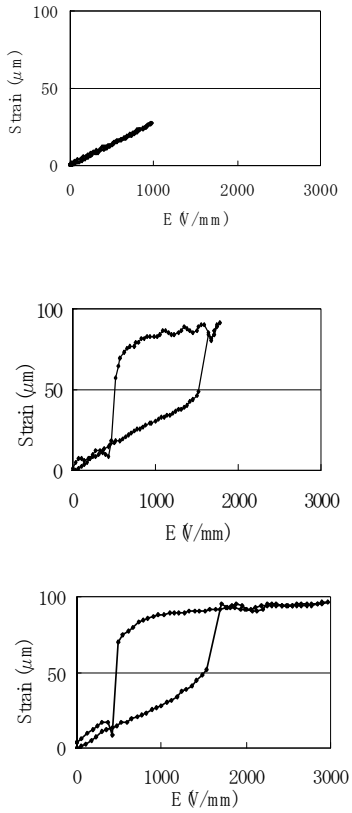


Fig. 25. Applied field (E) dependence of shrinkage strain in the length (13 mm) direction in PZNT91/09 single-crystal plate with giant k_{31}.

Figure 26 shows the Ti composition (x) dependence of E vs strain in PMNT(1-x)/x single-crystal plates measured at room temperature (pseudo-cubic phase) and under E=1500 V/mm. By increasing x from 0.251 to 0.299, the linear relationship between E and strain changed into a line with a brake, and finally reached to a typical E vs strain similarly to the case of PZT ceramics. Furthermore, the E of 800 V/mm to generate the triple and asymmetric loops corresponded to the E of a break in the line for E vs strain.

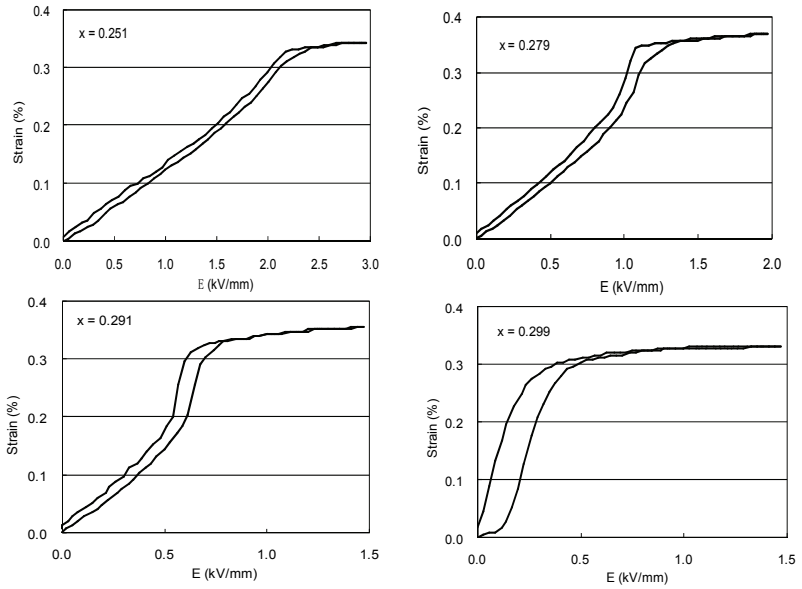


Fig. 26. Ti composition dependence (x) of E vs strain in PMNT(1-x)/x single-crystal plates; x=0.251(linear line and small hysteresis), x=0.279/ 0.291 (line with break and intermediate hysteresis) and x=0.299 (large hysteresis like PZT ceramics).

4.2.3 Field-induced phase transition

A mechanism to realize giant k_{31} can be explained using the crystal plane, which closely affects the direction of the spontaneous polarization, and poling direction. Giant k_{31} in relaxor single-crystal plates can be achieved when the poling field generates strain to move the ferroelectric domains in the plates ($13^{L}\times4.0^{W}$ mm) and not to only expand the spontaneous polarization axes in the direction of the poling field. Figure 27 shows the relationships between crystal planes, spontaneous polarization axes, and poling direction in (110) PMNT(1-x)/x single-crystal plates (x=0.251-0.301) in comparison with the case of (100) and (110) PZNT91/09 single-crystal plates. The crystal phases after poling can be estimated using the values of k_{31} and the combination between the directions of the spontaneous polarization axes and the poling field, which generates the strain to move the domains in the plates. Therefore, it was considered that the crystal phase of the PMNT(1-x)/x single-crystal plates after poling changed from pseudo-cubic to pseudo-cubic (x=0.251-0.262) from pseudo-cubic to orthorhombic (x=0.273-0.293), and from pseudo-cubic to rhombohedral (x=0.296-0.301), because of the combination to move the domains in the plates. These results were supported by the fact that the shapes of the P-E loops are triple or asymmetrical. Furthermore, it was considered that the E for such types of loops to appear was a coercive field to generate the DC-field-induced phase transition with giant k_{31}.

In conclusion of this part, the relationships between giant k_{31} (>80%) and k_{33} (>90%) in (100) PZNT91/09 and (110) PMNT(1-x)/x single-crystal plates were clarified to investigate the P-E hysteresis loops and the strain measurement. Triple and asymmetrical loops appeared in PMNT(1-x)/x single-crystal plates with giant k_{31} as well as in PZNT91/09 single-crystal plates with giant k_{31}. The typical relaxor-type hysteresis was observed for the electric-field-induced strain and their break points correspond to the coercive field to generate giant k_{31}. The crystal

phases after DC poling could be estimated using the relationships between the crystal plane, which closely affects the direction of the spontaneous polarization, and poling direction.

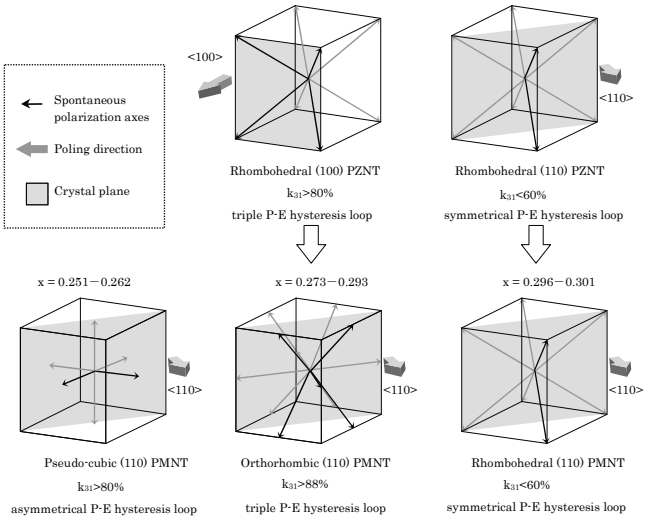


Fig. 27. Schematic diagrams of relationships between crystal plane, which affects direction of spontaneous polarization, and poling direction for realizing giant k_{31} (>80%) in (110) PMNT(1-x)/x (pseudo-cubic phase before poling) and PZNT91/09 (rhombohedral phase before poling) single-crystal plates at poling temperature of 40 °C.

5. Applications

Utilizing the giant k_{31} and d_{31} in PZNT91/09 single crystals, devices such as piezoelectric unimorphs and bimorphs were fabricated in comparison with the devices consisting of PZT ceramics.

5.1 Applications of $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ single-crystal plates with giant k_{31} to piezoelectric unimorphs and bimorphs

In this part, the piezoelectric and displacement properties on various kinds of unimorphs and bimorphs were reported. Piezoelectric unimorphs were prepared by sticking the PZNT91/09 single-crystal plates with giant k_{31} on center shim plates ($15^{L}x4^{W}x0.10^{T}$/ 0.20^{T} mm) composed of 42 nickel alloy. These were compared with unimorphs fabricated by ordinary PZT ceramic plates (k_{31}=37%, d_{31}=-330 pC/N) with the same dimensions. Furthermore, series-type bimorphs were made from the unimorphs by sticking other PZNT91/09 single-crystal plates and also PZT ceramic plates. The coupling factors on the bending mode (k_b) of the unimorphs and bimorphs were evaluated. The displacement of the devices was measured by laser displacement equipment at room temperature.

5.1.1 Realization of giant k_{31} over 80% in single-crystal plates

Table 4 shows the poling and annealing processes to obtain the giant k_{31} over 80%. When we poled three plate samples ($13^{L}x4^{W}x0.36^{T}$ mm) of Nos. 1~3, only the one sample of No. 3-1 had a giant k_{31} of 85.6%. The others were 42.2% (No. 1-1) and 40.4% (No. 2-1). Therefore, the

Sample No.	E (kV/mm)	k_{31} (%)	k_t (%)
1-1	1.0	42.2	55.1
	Annealing	0.0	0.0
1-2	1.0	49.6	59.0
1-3	1.5	39.6	55.8
1-4	2.0	79.5	56.2
1-5	2.5	55.7	59.6
1-6	3.0	39.8	55.7
2-1	1.0	40.4	54.9
	Annealing	0.0	0.0
2-2	1.0	45.4	54.2
2-3	1.5	86.2	56.2
3-1	1.0	85.6	56.8

Table 4. Process combination of poling and annealing to obtain Giant k_{31}.

annealing at 200 °C for 30 min was carried out to de-polarize the samples. On the following processes, the poling fields increased from 1.0 kV/mm to 3.0 kV/mm. As a result, the giant k_{31} was realized in the cases of No. 1-4 and No. 2-3 while the electromechanical coupling factors of the thickness mode (k_t) were almost the same of 54~60%. This means that the domain reorientation in thickness had been saturated; on the other hand, the one in the plate is changeable by the poling field. Furthermore, there was an optimum DC poling field for appearing the giant k_{31} on each individual plate sample. As mentioned above, the giant k_{31} can be obtained by the process combination of the DC poling and the annealing. Figure 28

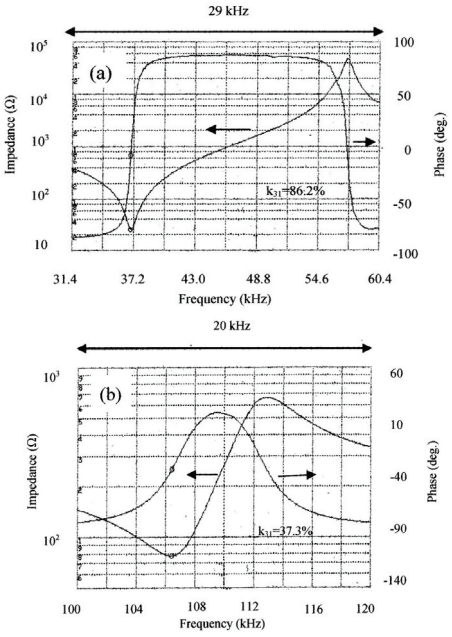


Fig. 28. Frequency responses of impedance on k_{31} mode in (a) PZNT91/09 single-crystal plate and (b) PZT ceramic plate.

shows the comparison between frequency responses of impedance in (a) the PZNT91/09 single-crystal plate and (b) the conventional PZT ceramic plate. The k_{31}'s were 86.2% (PZNT91/09: sample No. 2-3 in Table 4) and 37.3% (PZT), respectively.

5.1.2 Bending mode prpperties

The PZNT91/09 single-crystal plate (13^{L}x4.0^{W}x0.36^{T} mm) with giant k_{31} of 86.2% (No. 2-3 in Table 4) was stuck on a center shim plate (15^{L}x4^{W}x0.20^{T} mm) composed of 42 nickel alloy to prepare a piezoelectric unimorph. The same dimensions of the PZT ceramic plate (k_{31}=37%, d_{31}=-330 pC/N) was also used to realized a unimorph. Figure 29 shows the comparison between frequency responses of impedance in (a) the PZNT91/09 single-crystal unimorph and (b) the conventional PZT ceramic unimorph. The k_b=64.7% on bending mode in the PZNT91/09 single-crystal plate was three times larger than the k_b=20.6% in the PZT ceramic plate. Therefore, it was confirmed that the giant k_{31} and d_{31} constant could be useful to realize the piezoelectric unimorphs with high efficiency as well as the plate (13^{L}x4.0^{W}x0.36^{T} mm) resonators with giant k_{31} and d_{31} constant.

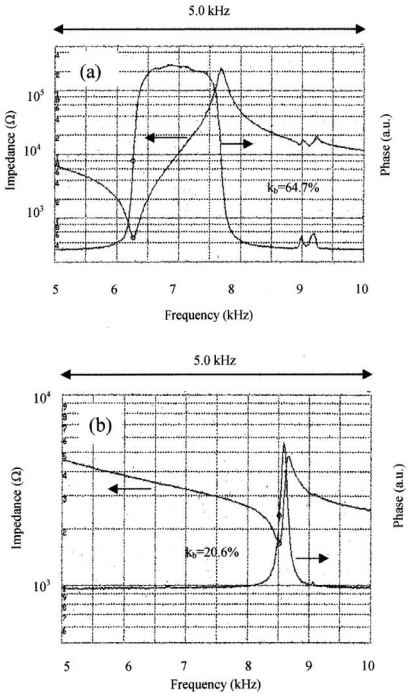


Fig. 29. Frequency responses of impedance on k_b mode in (a) PZNT91/09 single-crystal unimorph and (b) PZT ceramic unimorph.

A piezoelectric bimorph was fabricated by sticking the PZNT91/09 single-crystal plate with giant k_{31} of 85.6% (No. 3-1 in Table 4) on the PNZT91/09 single-crystal unimorph with the k_b of 64.7% as previously mentioned. A PZT ceramic bimorph was also prepared. Figure 30 shows the comparison between frequency responses of impedance in (a) the PZNT91/09

single-crystal bimorph and (b) the conventional PZT ceramic bimorph. The k_b=69.8% on bending mode in the PZNT91/09 single-crystal plate was twice larger than k_b=31.2% in the PZT ceramic plate. Therefore, it was confirmed that highly efficiency piezoelectric devices could be realized to utilize PZNT91/09 single-crystal plates with giant k_{31} and d_{31} constant in the cases of the piezoelectric bimorphs as well as the piezoelectric unimorphs.

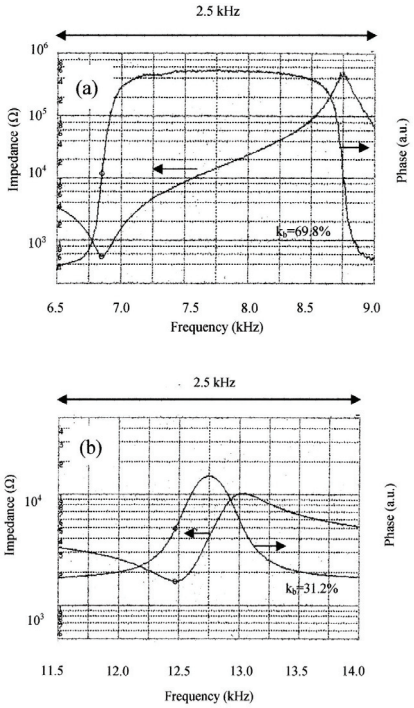


Fig. 30. Frequency responses of impedance on k_b mode in (a) PZNT91/09 single-crystal bimorph and (b) PZT ceramic bimorph.

5.1.3 Displacement properties

The displacement was evaluated regarding the PZNT91/09 single-crystal unimorphs (the center shim plate thickness of 0.20 mm)/ bimorphs (the center shim plate thickness of 0.10 mm) and the PZT ceramic unimorphs (the center shim plate thicknesses of 0.10 mm and 0.20 mm)/ bimorphs (the center shim plate thickness of 0.10 mm). In the case of a series-type bimorph in Fig. 31, the total displacement (u =a+b) was estimated by the following equation;

$$u = \left(\frac{3}{2} d_{31} \left(\frac{l}{t} \right)^2 \cdot \left(1 + \frac{t_s}{t} \right) V\alpha \right) \times 2 \tag{1}$$

where l : effective length (9 mm), t : thickness of devices (0.36+0.2 mm for single-crystal and ceramic unimorphs, 0.36+0.1 mm for ceramic unimorph, and 0.36x2+0.1 mm for single-

crystal and ceramic bimorphs), t_s : thickness of shim plate (0.1 mm and 0.2 mm), V : applied voltage and α : non-linearity coefficient, respectively.

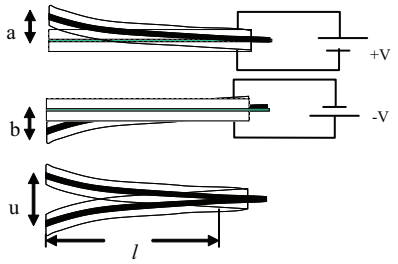


Fig. 31. Series type bimorphs and total displacement.

The relationships between the applied voltage and the displacement were shown in Fig. 32 for the different shim thickness in the PZNT single-crystal unimorph and the PZT ceramic unimorph. The d_{31} constants of the stuck piezoelectric plates calculated from the frequency responses of the impedance were -2020 pC/N in the PZNT91/09 single crystal and -330 pC/N in the PZT ceramics, respectively. The displacement of the PZNT91/09 single-crystal unimorph was twice larger than the one of the PZT ceramic unmorph. The decrease in thickness of the shim plate from 0.20 mm to 0.10 mm increased the displacement in the range of over 100 V. The α calculated from (1) was 0.4~0.5 in the PZNT91/09 single-crystal unimorph. Otherwise, the α was 1.0 (≦100 V) and 1.6 at 180 V in the PZT ceramic unimorph. Furthermore, the α was independent of the shim plate thickness in the PZT ceramic unimorphs.

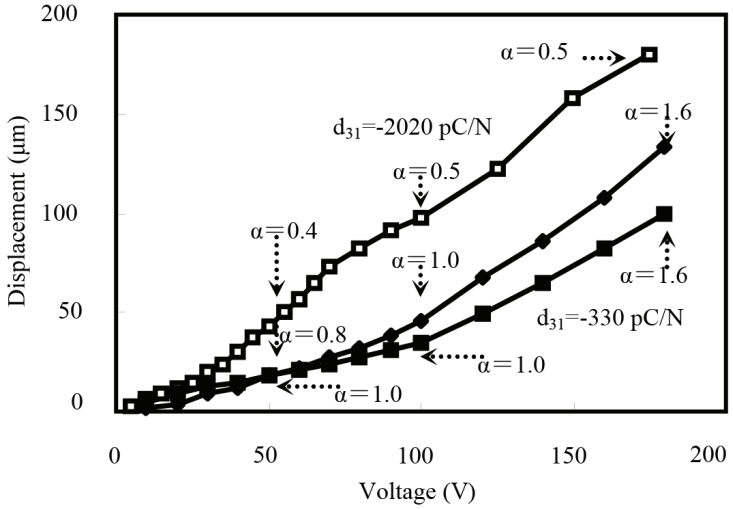


Fig. 32. Applied voltage dependence of displacement in PZNT91/09 single-crystal unimorph (□: shim thickness of 0.20 mm) and PZT ceramic unimorph (■: shim thicknesses of 0.20 mm and ◆: 0.10 mm).

Figure 33 shows the applied voltage dependence of the displacement in the PZNT91/09 single-crystal bimorph and the PZT ceramic bimorph. The average d_{31} constants of the two stuck PZNT91/09 single-crystal plates and the two stuck PZT ceramic plates also showed in this figure. Although the d_{31} constant of the PZNT91/09 single crystals is 4~7 times larger than the d_{31} of the PZT ceramics, the displacement of the PZNT91/09 single-crystal bimorph became almost twice larger than the one of the PZT ceramic bimorph. The reason the displacement becomes twice, not more, was due to that the α in the PZNT91/09 single-crystal bimorph was a half of the α in the PZT ceramic bimorph.

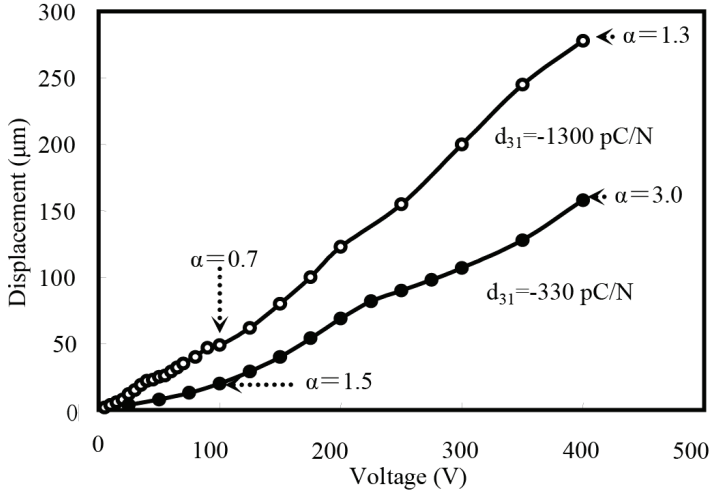


Fig. 33. Applied voltage dependence of displacement in PZNT91/09 single-crystal bimorph (○: shim thickness of 0.10 mm) and PZT ceramic bimorph (●: shim thickness of 0.10 mm).

The origin of the decrease in α of the PZNT91/09 single-crystal bimorph was thought the mechanical softness of PZNT91/09 single-crystal plates with giant k_{31} and d_{31} constant. Namely, the Young's modulus of PZNT single crystals (0.89×10^{10} N/m) is one order smaller than the one of PZT ceramics ($6 \sim 8 \times 10^{10}$ N/mm). In addition to the above mentioned, the values of α in bimorphs were approximately twice larger than the ones of unimorphs. This phenomenon was thought that the α depends on the number of the piezoelectric plate; one plate in unimorph and two plates in bimorph, respectively.

In conclusion of this part, the process combination of poling and annealing to obtain giant k_{31} and d_{31} constant was clarified to fabricate PZNT91/09 single-crystal unimorphs and bimorphs. The coupling factors on bending mode (k_b) in PZNT91/09 single crystal unimorphs and bimorphs were 2~3 times larger than the k_b's in PZT ceramic unimorphs and bimorphs. The displacement of PZNT91/09 single-crystal unimorphs and bimorphs was almost twice larger than the one of PZT ceramic devices. The advantage of PZNT91/09 single-crystal plates with giant k_{31} and d_{31} constant was confirmed through the development of piezoelectric devices such as unimorphs and bimorphs.

6. Conclusion

We found the giant electromechanical coupling factor of k_{31} mode to be over 80% and the piezoelectric d_{31} constant to be nearly -2000 pC/N in ferroelectric relaxor single-crystal plates. The discovery of the giant k_{31} and the d_{31} constant became breakthroughs in applications to high-performance sensors and actuators utilizing k_{31} mode.

7. Acknowledgments

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8. References

Koto, R. et al. (2006). Chemical Composition Dependence of Giant Piezoelectricity on k_{31} Mode in $Pb(Mg_{1/3}Nb_{2/3})O_3$–$PbTiO_3$ Single Crystals, *Jpn. J. Appl. Phys.*, Vol.45, pp. 7418-7421.

Koto, R. & Ogawa, T. (2007). Frequency Response Analysis by Finite Element Method in Relaxor Single-Crystal Plates with Giant k_{31}, *Jpn. J. Appl. Phys.*, Vol.46, pp. 7058-7062.

Kuwata, J. et al. (1982). Dielectric and Piezoelectric Properties of $0.91Pb(Zn_{1/2}Nb_{2/3})O_3$-$0.09PbTiO_3$ Single Crystals, *Jpn. J. Appl. Phys.*, Vol.21, p. 1298-1302.

Matsushita, M. et al. (2001). *Abstr. Am. Ceram. Soc., 103rd Annual Meet.*, p. 247.

Ogawa, T. & Nakamura, K. (1999). Effect of Domain Switching and Rotation on Dielectric and Piezoelectric Properties in Lead Zirconate Titanate Ceramics, *Jpn. J. Appl. Phys.*, Vol.38, pp. 5465-5469.

Ogawa, T. et al. (2002). Giant Electromechanical Coupling Factor of k_{31} Mode and Piezoelectric d_{31} Constant in $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ Piezoelectric Single Crystal, *Jpn. J. Appl. Phys.*, Vol.41, pp. L55-L57.

Ogawa, T. & Numamoto, Y. (2002). Origin of Giant Electromechanical Coupling Factor of k_{31} Mode and Piezoelectric d_{31} Constant in $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ Single Crystal, *Jpn. J. Appl. Phys.*, Vol.41, pp. 7108-7112.

Ogawa, T. et al. (2005). Giant Piezoelectricity on k_{31} Mode in $Pb(Mg_{1/3}Nb_{2/3})O_3$–$PbTiO_3$ Single Crystal, *Jpn. J. Appl. Phys.*, Vol.44, pp. 7028-7031.

Ogawa, T. (2005). Piezoelectric Bimorph with Giant Electromechanical Coupling Factor of Bending Mode Nearly 70% Fabricated by Low Symmetry Mono-Domain $Pb[(Zn_{1/3}Nb_{2/3})_{0.91}Ti_{0.09}]O_3$ Single Crystal, Ferroelectrics, Vol.320, pp. 115-123.

Ogawa, T. (2008). Giant Transverse-Mode Electromechanical Coupling Factor and Piezoelectric Strain in Relaxor Single-Crystal Plates Evaluated Using P-E Hysteresis Loop, *Jpn. J. Appl. Phys.*, Vol.47, pp. 7655-7658.

Yin, J. et al. (1999). *IEEE Proc. Med. Imag.*, Vol.3664, p. 239.

2

MEMS Based on Thin Ferroelectric Layers

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1. Introduction

Micro-Electro-Mechanical Systems (MEMS) are devices that display the most intense development in modern microelectronics (Kostsov, 2009).
The main challenge of microelectromechanics is the design of unique micromechanical structures for various purposes. This research direction is based on achievements of advanced microelectronic technologies and inherits the basic advantages of electronic microchips: high reliability and reproducilbility of characteristics, low cost, and large scales of applications (Esashi & Ono, 2005). The essence of micromechanics implies that advanced microelectronic technologies, for instance, deep etching of silicon (or silicon-on-insulator (SOI)) make it possible to create integrated circuits (ICs) simultaneously with micromechanical structures with unique parameters (determined by their microscopic or nanoscopic sizes, with the transported mass being 10^{-4} to 10^{-18} g) controlled by electronic circuits.
The most important feature of MEMS is the precision fabrication of moving elements of mechanical structures (earlier inaccessible in mechanics) and their unification in one technological cycle with controlling and processing electronic elements created on the basis of CMOS technology.
MEMS applications include the following areas (Kostsov, 2009):

- microoptoelectromechanics (displays, adaptive optics, optical microswitches, fast-response scanners for cornea inspection, diffraction gratings with an electrically tunable step, controlled two- and three-dimensional arrays of micromirrors, etc.);
- high frequency (HF) devices (HF switches, tunable filters and antennas, phased antenna array, etc.);
- displacement meters (gyroscopes, highly sensitive two- and three-axial accelerometers with high resolution, which offer principally new possibilities for a large class of electronic devices);
- sensors of vibrations, pressures, velocities, and mechanical stresses; microphones (there are millions of them in cellular phones). Back in 2004, Intel started to deliver RF front-end assemblies fabricated by the MEMS technology for cellular phones. They integrate approximately 40 passive elements, which allows the producer to save up to two thirds of space in the phone casing;
- wide range of devices for working with microvolumes of liquids and for applications in biology, biochips, biosensors, chemical testing, creation of a new class of chemical sensors, etc.;
- microactuators and nanopositioners; microgenerators of energy.

Many experts think that the telecommunications market is one of the promising areas of MEMS implementation, including the technologies related to optical switches for fiber-optical telecommunications systems.
It becomes obvious that none of the fields of modern electronic engineering will avoid the touch of the new industrial revolution.
The basic component of most micromechanical devices is the energy converter, namely, micromotor (or microactuator). Therefore, the main attention in this work is paid to the analysis of the operation of new micromotor proposed by us, the examples of the micromotor application in MEMS devices are presented at the end of the chapter.
There are electromagnetic, electrothermal, piezoelectric and electrostatic effects among the variety of physical principles basic for these converters.
Presently, there are two common kinds of the motors (the devices that convert electrical energy into the mechanical motion): induction motors (IM) and electrostatic motor (EM). Classic electrostatic motors are not widely used mainly because it is necessary to use high operating voltage to achieve the specific energy output comparable with IM motors. At the same time, the specific energy output of the IM decreases as their power becomes small, and this decrease starting from power of 10-100 mW makes induction micromotors ineffective.
The advantages of the capacitance (EM) machines over IM machines in the low power domain can be attributed to the main difference between the electric and magnetic phenomena: the existence of electric monopoles and the absence of magnetic ones. To create an electric field in the operating gap of the capacitance devices it is enough to have a small amount of the conductive matter. At the same time, to create magnetic field in the operating gap of the induction machines it is necessary to have large amounts of ferromagnetic matter in the form of large magnetic conductor that is used to create opposite magnetic charges at the ends of the gap. This magnetic conductor is the reason for the low energy output of the small energy capacity induction machines.
The parameters of the capacitance electromechanical devices such as driving force, power, reaction time with respect to voltage pulse can be improved by the increase in the field strength in the gaps, as they are proportional to the energy density of the field $\varepsilon\varepsilon_0 E^2/2$, where ε and ε_0 are the dielectric permeabilities of the medium and the vacuum.
Use of the micromachining for the manufacturing of the electrostatic micromotors allows one to reach significantly smaller gaps (on the order of several micrometers), and to get higher values of electric field strength and energy density (Harness& Syms, 2000; Wallrabe et al.,1994; Zappe et al., 1997; Kim & Chun, 2001).
The estimates of specific energy output based on the energy density of electric and magnetic fields can be used to determine the gap width necessary for the electric field energy density to be comparable to or higher than magnetic field energy density (~$4\text{-}5\cdot10^5$ J/m^3 with 1 T induction and very high quality of magnetic material). For 20-60V voltage, the gap is 2 μm. Such a gap that is used in modern electrostatic micromotors results in the higher value of the electric energy stored in the sample, as compared to the classical electrostatic motors, and, consequently, in the better motor efficiency.
With the help of silicon deep etching technology the gaps of about 2 μm can be created, so the specific electric capacitance C_{sp} and specific energy output A_{sp} of the elemental actuator can be as high as 4 pF/mm^2 and 10^{-8} J/mm^2 respectively, and the driving force F can achieve the value of 10^{-6}- 10^{-5} N.
The processibillity in fabrication of electrostatic motors, the simple design and no need to use the magnetic core are the reasons for the dominant use of the electrostatic microactuators in MEMS.

The operation principle of these microactuators is as follows: the moving electrode is pulled in the interelectrode gap with the pulling force equal to $(V^2\partial C/\partial x)/2$ (V is applied voltage, C – total capacitance of the structure). The drawbacks of these microactuators are the small values of the main parameters C_{sp}, A_{sp}, F and the small range of moving element (moving platform, MP) motion – on the order of 5 – 50 μm. To increase the power of the device it is necessary to use many microactuators in parallel and, consequently, use a significant part of the integrated circuit surface. The forces developed by these micromotors are in the range of 1 – 10 μN. This value determines the field of the micromotor applications.

A certain increase of C_{sp}, not more than by one order of magnitude, can be achieved by filling the interelectrode gap by dielectric. The techniques of such energy conversion were proposed in papers (Dyatlov, et.al., 1991; Dyatlov, et.al., 1996; Sato & Shikida, 1992; Akiyama & Fujita, 1995).

On the other hand the thin-film metal-ferroelectric-metal structures have high enough electrical power capacity, which can exceed the corresponding capacity of air gap by thousand times due to high values of ε at higher breakdown strength. To convert even a part of this energy into mechanical one we have use the effect of reversible electrostatic attraction of thin metal films to the surface of ferroelectrics under action of electric field, so called „electrostatic glue".

2. "Electrostatic glue"

The object of study was thin-film structures of a new type synthesized on the surfaces of silicon or sapphire substrates and composed of a ferroelectric film with a high permittivity ε and thickness d and an elastic mobile thin electrode with an air nanogap of thickness d_z between (fig. 1).

The ferroelectric component was a strontium barium—niobate (SBN) film doped with lanthanum ($Ba_{0.5}Sr_{0.5}Nb_2O_6$ + 1% La) and with a permittivity of 3000—5000. The film was synthesized on an ITO (In_2O_3 + 6% SnO_2) electrode surface. The thicknesses of the ITO and SBN films were 0.1—0.5 and 0.3—3 μm, respectively. The preparation technique of the films and their main electrical characteristics were described in (Kostsov, 2005).

During the electrostatic attraction of the petal to the ferroelectric surface the total current consisting of the conductive current and the capacitance current arises in the electric circuit. Our technique allows us to separate these components during in real time.

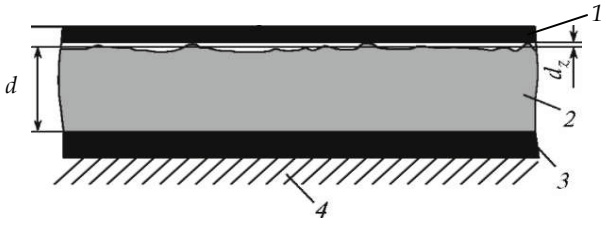


Fig. 1. Schematic diagram illustrating the electrostatic pressing of a metal film (1) to the surface of ferroelectric film (2), deposited on a substrate (4) with a barrier electrode (3)

The voltage pulse applied to the structure was modulated by sine voltage with the frequency equal to 1 MHz and the amplitude equal to 1 – 2% of the total pulse amplitude V. The response to this voltage pulse allows one to measure alternating conduction (in-phase signal) and capacitance (signal shifted by 90°) current, and then one can calculate the transient values of conductivity and capacitance C(t).

Study of C(t) behavior during the electrostatic pressing of the metal and the ferroelectric surfaces performed on the prototype consisting of the large petal (l=10 mm in length and b=1 mm in width) freely lying on the surface of the ferroelectric film (see fig.2) shows that as V grows, the process duration abruptly drops. The C(t) values initially grows, and then comes to the saturated value that is determined by the width of the air gap between the metal and the ferroelectric and the parameters of the BSN film. As V grows further, saturated value of C(t) can fall because the capacitance of ferroelectric layer becomes smaller due to the polarization screening in the ferroelectric. To reduce this effect of polarization charge accumulation it is necessary to apply shorter pulses, use shorter petals and apply bipolar voltage pulses (Baginsky & Kostsov, 2004). With l equal to 1-3 mm pulse duration t_p should be between 50 –500 μs.

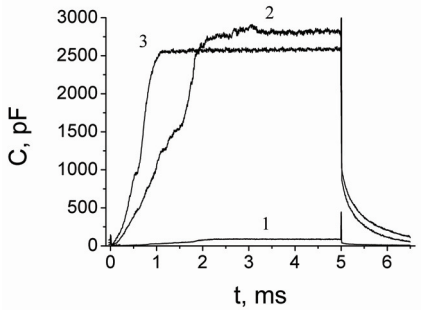
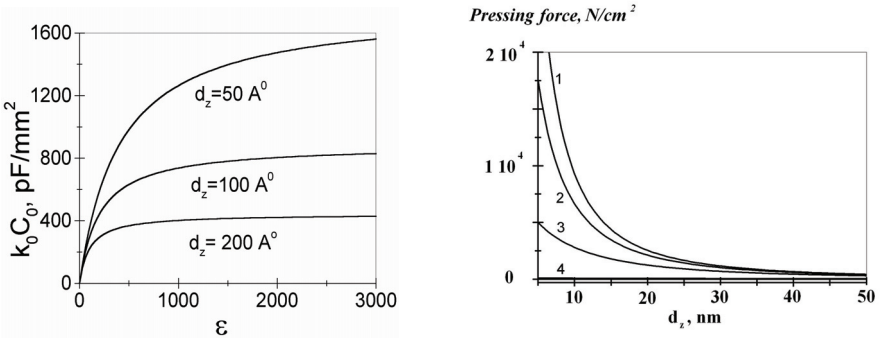


Fig. 2. Time behaviour of the capacitance of the free lying petal – BSN film (d=2.4 μm) – electrode structure when a voltage pulse with duration of t_p=5 ms and amplitude V= **1** – 30, **2** – 40, **3** – 50 V is applied.

Due to the high ε value, the electric field in the structure under a voltage V is such that the potential drops mainly on the air gap between the mobile electrode and ferroelectric film; i.e., the field is mainly concentrated in the gap, and the specific capacitance of the structure $C_{sp}=k_oC_o$ is several times less than the specific capacitance C_o of the metal-ferroelectric-metal (MFM) structure with the applied electrodes. At sufficiently high values of ε/d the value of C_{sp} approaches to the gap capacitance C_Z, and the experimental studies show that k_o can be about 0.05 – 0.5, see fig. 3a. The field redistribution between the ferroelectric and air gap may occur only at high ε values (specifically, when $\varepsilon/d > 10^8$ m^{-1} (Kostsov, 2008)). Analysis of the field distribution in the air gap for different ε/d values shows that, with a decrease in d_z, the pressing force $F_p=V^2(dC_z/dz)$ for the mobile electrode to the ferroelectric surface nonlinearly increases (fig. 3b). The force significantly increases beginning from a distance of 100 nm or less between the surfaces, and at $\varepsilon/d > 10^9$ m^{-1} one can obtain a pressure of more than 10^4 N/cm^2 in the nanogap. Note that for the linear dielectrics ($\varepsilon/d < 10^7$ m^{-1}) the voltage drop on the nanogap is insignificant. Although the voltage applied to the nanogap is fairly high (up to 100 V or more), it does not cause electric breakdown, because (i) the Paschen law is invalid for such narrow air gaps and (ii) in this structure the ferroelectric film resistance more than 10 MOhm/mm^2 is connected in series with the gap. The breakdown field strength of the ferroelectric film exceeds 100 V/μm, and a low voltage drop directly on the ferroelectric film excludes its breakdown.

The air nanogap width d_z determined by measuring the total capacitance of the structure is falling with an increase in the voltage applied. For a specific sample, the minimum d_z value



a. b.

Fig. 3. The dependence of specific capacitance on dielectric permittivity value for the system: free metal film-ferroelectric film-electrode for various values of air gap d_Z (**a**): d=2 μm and the pressing force on d_Z value (**b**): ε/d= (1)-10^9, (2)-3.3 10^8, (3)-10^8, (4)-$10^7 m^{-1}$.

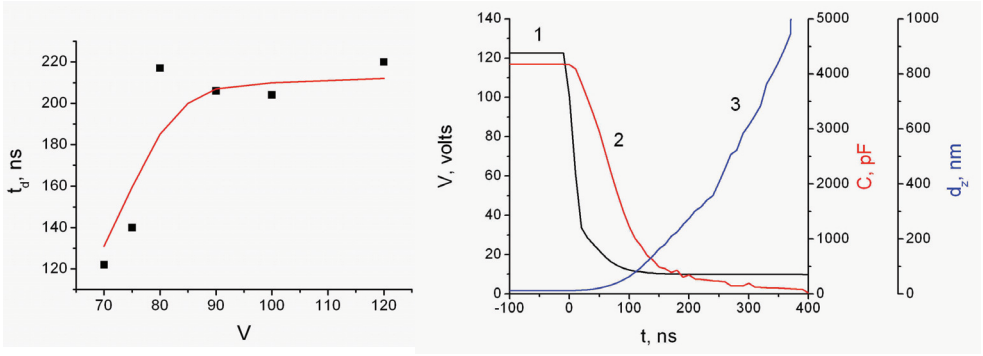
is limited by the roughness of the surfaces of both the ferroelectric film and mobile electrode and the specific capacitance C_{sp} of the structure at the instant of pressing the mobile electrode is $10—10^3$ pF/mm², depending on V.

It was found experimentally that the adhesion force of the electrostatically pressed (using electrostatic "glue") surfaces depends linearly on the electrostatic energy accumulated in the structure and exceeds (3—5) x 10^5 N/J. In particular, a force above 10 N is necessary to separate surfaces 1 cm² in area. The pressure in the nanogap may exceed 10^4 N/cm²; it is determined by the crystal quality of the ferroelectric film and its hardness.

Note that in this case the pressure formed by the electric field in the nanogap greatly (by orders of magnitude or even more) exceeds the pressure obtained in the gaps of large modern devices using stationary magnetic fields close to the maximally possible (to (3—4) x 10^6 A/m). In this case, the decisive factor is the field energy density $\varepsilon\varepsilon_0 E^2/2$ or $\mu\mu_0 H^2/2$ ($\mu\mu_0$ is the magnetic permeability, H – magnetic field strength), which is measured in J/m³ and identically equal to pressure in N/m². In the case considered here E may reach values up to 10^{10} V m^{-1} and, correspondingly, the energy density can be as high as 4 x 10^8 J/m³ (pressure up to 10^5 N/cm²).

We studied the specific features of breaking adhesion of the ferroelectric and metal film surfaces when switching off the voltage. It was established that the time of detachment of the mobile electrode from the ferroelectric surface lies in the nanosecond range (fig. 4a). Such a short detachment time is explained by the existence of two oppositely directed forces on the mobile electrode: the electrostatic force in the gap, formed by the applied voltage V, and a mechanical force, the origin of which is as follows: when the free thin metal film is electrostatically pressed against the ferroelectric surface, a significant part of the energy accumulated in the structure (estimated to be $10^{-3}— 10^{-2}$ J/m² or 1—5% of the electrostatic field energy) is spent on the elastic mechanical deformation of the metal film (beryllium bronze), which is pulled like a membrane on individual microasperities of the ferroelectric surface. The parameters of ferroelectric film surface roughness (the number and height of microasperities) are determined by the preparation conditions and film thickness. After switching off the voltage, the released mechanical energy determines the high detachment rate of the metal film (whose mass is $10^{-9}—10^{-10}$ g) from the ferroelectric surface for 50—200 ns. It is facilitated by the low space charge in the ferroelectric film and high surface hardness of the ferroelectric (5.5 on the Mohs scale).

To analyze how the surfaces are separated, we investigated the dependence of the structure capacitance relaxation (fig. 4b, curve 2) at a sharp drop of voltage pulse (the trailing edge of which was about 30 ns) from the initial amplitude V a small value V_1 (fig. 4b, curve 1), at which the metal film cannot be retained by electrostatic forces on the ferroelectric surface. We took into account that the conduction currents through the structure are negligible in comparison with the capacitance discharge current.
The effect considered here, see also (Baginsky & Kostsov, 2010), makes it possible to generate and remove strong forces of reversible adhesion between two surfaces at high clock frequencies, and it is the basic for the creation new type of micromotors and other MEMS devices.



a. b.

Fig. 4. Separation of the surfaces of a free metal film and ferroelectric at switching off of the voltage pulse (for the structure mobile metal film (beryllium bronze, 1.3 μm)- SBN film (2.4 μm)- electrode): (a) the dependence of the surface separation time on the voltage pulse amplitude and (b) separation of the metal film and ferroelectric film surfaces at switching off of voltage: (1) V(t), (2) C(t), and (3) $d_z(t)$.

3. Effect of rolling and the principle of micromotor operation based on this effect

The effect of rolling is a certain kind of electrostatic attraction of thin metal film, named below as a petal, at which the attraction is expanding gradually part by part from one end of the film to another.
The petal moving under the effect of the electrostatic force along the ferroelectric surface can transfer the motion to the external object (moving plate) upon bending, and thus carry out the electromechanic energy conversion. The movement velocity of the petal part that is rolled on the ferroelectric and the accumulated energy (transferred into mechanic energy) are defined by the voltage amplitude, ferroelectric film thickness and ε value. The evaluations show that the pressure in the interelectrode gap at the instant of the contact of the two surfaces (starting from the distance 10 nm) is equal to 10^4 – 1.5 10^4 N/cm^2 and the strain force of the metallic film can be as high as 100 N/mm^2 and more.
The schematic of the use of the electrostatic rolling for the conversion of the electric energy accumulated in the ferroelectric into the kinetic energy of the substrate motion is shown on fig.5.

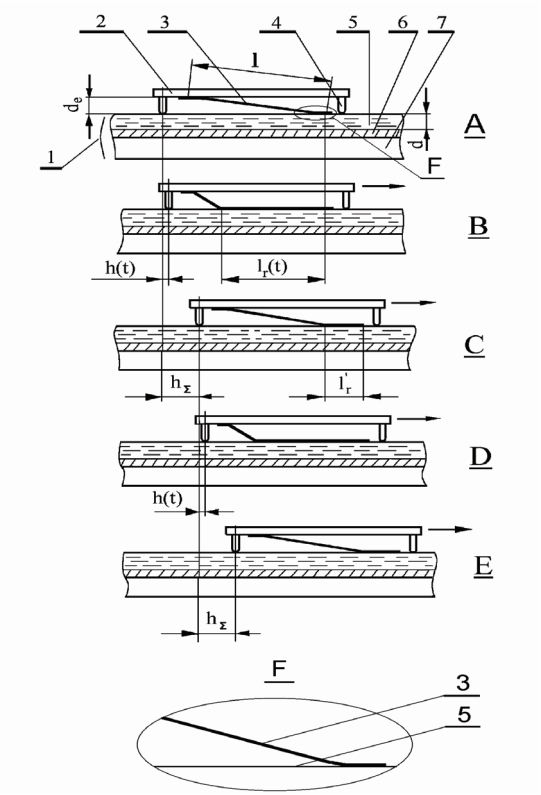


Fig. 5. A scheme illustrating for the motion effects for the petal micromotor. **A –** initial state and position, t = 0; **B –** the state and position at the end of the first voltage pulse, t = t_p; **C –** the state and position, corresponding to the t = T=1/f; **D –** the state and position at the end of the second pulse; **E –** the state and position, corresponding to the time t = 2T. The initial form of the petal at the contact with the surface of stator is shown in view **F**.

The stationary plate (stator) 1 consists of the silicon substrate 7, with the electrode 6 and ferroelectric film 5 applied to its surface. Petals 3 of length l are attached to the moving plate (slider) 2 that is located at the distance d_e from the stator. Slider moves with respect to stator along the guides 4. In the initial state A the ends of the petals are mechanically pressed to the stator surface, which facilitates the subsequent electrostatic adhesion (see view F). The motion consists of the several stages.

When the voltage pulse is applied between the petal 3 in its initial state A and the electrode 6, the electrostatic adhesion of the petal's end 3 and the ferroelectric film 5 takes place. Then the motion of the plate 2 starts because larger part of the petals' surface is rolled on the ferroelectric surface, and the petals are bent and mechanically stretched. Thus, the electromechanic energy conversion takes place. The rolling length $l_r(t)$ grows with the voltage pulse action time t. Therefore, the shift of the slider h(t) grows too. h(t) value and the speed of the petal's part that is being rolled on the ferroelectric depend on the mass m of the slider, the duration of the voltage pulse t_p, it's amplitude V and the friction coefficient k.

Force F that causes the motion of the slider is applied along the free (not pressed to the stator surface) part of the petal, fig.6. The tangential component of this force F_1 is the driving force, and the normal component F_2 increases the pressure between the slider and the guides. For the efficient energy conversion d_e/l ratio should be sufficiently small, less than 0.1 –0.2.

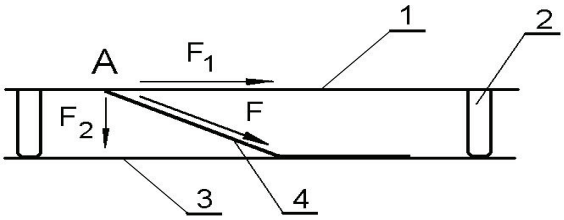


Fig. 6. A scheme illustrating for the pulling force application. 1 – moving plate, 2 – guides, 3 – stator, 4 – petal. A is the point of the force application.

After the end of the voltage pulse the elastic forces bring the petal either to the initial state A (with the single voltage pulse) or to the intermediate state C typical for the continuous movement of the slider (when a series of pulses with the frequency f is applied to the sample). During this time, inertia causes slider to travel the distance h_{Σ}. The time necessary to separate the petal from the ferroelectric surface and to bring petal to the initial shape defines the space between the voltage pulses and, consequently, the maximum pulse frequency and the motor power.
When the second pulse is applied to the sample, the plate makes one more step and comes to the state D. After the end of the second pulse, the slider comes to the state E because of inertia. With the third and further pulses the moving pattern is similar – from position B to position C, etc.

4. Numeric modeling of the electrostatic rolling

To analyze the operation of the linear micromotors in the step regime the mathematical model of the electrostatic rolling was developed based on the energy balance (Dyatlov& Kostsov, 1998, 1999). The redistribution of the electric energy accumulated in the structure during the electrostatic rolling between the kinetic energy of the slider, the work of the load force of the motor (friction) and the petal deformation energy A_d is considered. The parameters of the model are the dimensions of the petal, the Young modulus of the petal material, the motor characteristics (d_e, m, k values), and the voltage source characteristics (t_p, V).
The specific energy of the electrostatic rolling a_r is defined as $a_r = k_o C_o V^2/2$, where $k_o C_o = C_{sp}$.
The work of the electrostatic rolling can be expressed as $A_r = a_r S_r$, where $S_r = b\, l_r(t)$ is the rolling area of the petal during the voltage pulse action. A_r is distributed between the kinetic motion energy, friction force work (effective load) and the deformation energy of the metallic film A_d:

$$A_r = \frac{m}{2}\left(\frac{dh}{dt}\right)^2 + \int_0^h F(x)dx + A_d\,, \tag{1}$$

where x axis coincides with the motion direction. In the first approximation, the shape of the bent part of the petal is described by the cubic parabola with the smooth contact between the petal and the ferroelectric surfaces, see fig. 7.

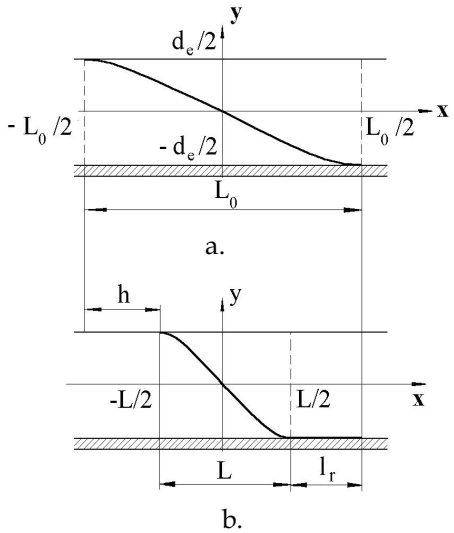


Fig. 7. A scheme for the designations of mathematical model. (**a) –** initial state of the petal, (**b) –** some intermediate state in the process of rolling.

Fig.8 shows the curves characterizing the typical behavior of the single petal motor during the single voltage pulse for 4 different loads. Fig. 8a shows the load force F, fig.8b – the rolling length l_r, fig.8c shows the rolling speed, and fig.8d shows the step h. Other parameters are: L_0 = 4 mm (see fig.7), b = 1 mm, d_e =0.2 mm, k = 0.2, a_r = 0.3 J/m^2, which corresponds to C_{sp} equal to1000 pF/mm^2 at V = 24.5 V.

This figure shows that right after the start of the voltage pulse the motor develops the highest motive force, up to 1-10 N per 1 mm^2 of the rolling area. This force drops later, because as the slider moves the petal tension decreases. The higher the load the more efficiently is the electrostatic rolling energy used. Thus, for the efficient electrostatic rolling energy utilization, t_p value has to be optimally adjusted for the load.

After the end of the voltage pulse the slider continues to move because of inertia, and at a certain time t_{st} determined by the friction coefficient and the slider speed it comes to rest.

The acceleration of the slider depends on its mass and it can be as high as 10000 g when the slider mass is equal to the mass of the petal.

The conversion of the electrostatic rolling energy into different forms of energy for the two different loads (0.1 and 10 grams, respectively) is shown on fig. 9 (a and b). Here the curve 1 describes the increase in the total energy use from the external source during the electrostatic rolling. Curve 2 shows the kinetic energy $mv^2/2$ (v is the slider speed), curve 3 – the energy spent to overcome friction, curve 4 – the work necessary to bend the petals (the work against the elasticity forces). The energy redistribution is time-dependent, the nature of this redistribution is defined by the motor parameters. The parameters can be optimized in such a way that 80-90% of the electric energy will be converted into mechanic energy of the slider

motion. The energy spent on the petal bending will be small, and the electrostatic forces would mainly act to stretch the petals. The estimates show that the stretch forces are much less than the elastic limit of the material. The bending deformation is potentially more serious, but, if the moving plate is sufficiently loaded, it is small, too. Thus, despite the small thickness of the petals, the motor can develop high forces without irreversible petals deformation.

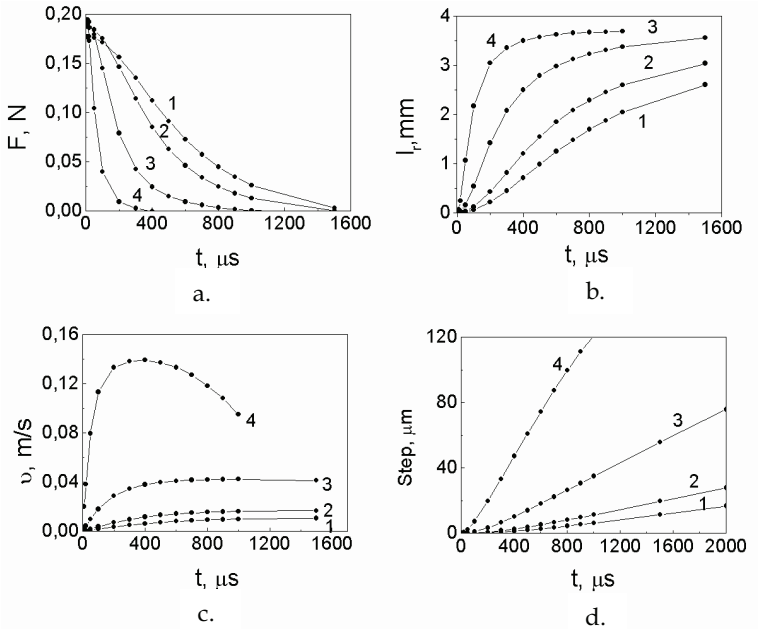


Fig. 8. The theoretical dependencies on the single voltage pulse duration of the following characteristics: (**a**) - traction force, (**b**) - rolling length, (**c**) and (**d**)- velocity and step of micromotor, respectively. m=50, 10, 1 and 0.1 g for curves 1, 2, 3 and 4, respectively.

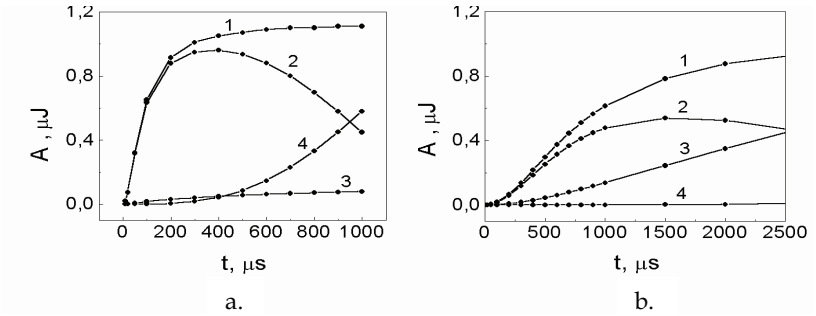


Fig. 9. Energies redistribution in the process of rolling for two different loads: m = 0.1 and 10 grams for figs. **a** and **b**, respectively. Here the curve 1 describes the increase in the total energy use from the external source during the electrostatic rolling. Curve 2 shows the kinetic energy $mv^2/2$, curve 3 – the energy spent to overcome friction, curve 4 – the work necessary to bend the petals (the work against the elasticity forces).

5. Studied structures

Each of the studied samples consisted of the two substrates with the 100-200 μm gaps. The lower (silicon) substrate was stationary one. Metallized ITO and $Ba_{0.5}Sr_{0.5}Nb_2O_6$ ferroelectric films were subsequently deposited by the RF-sputtering on the stationary substrate. The ferroelectric used was barium-strontium niobate ($Ba_{0.5}Sr_{0.5}Nb_2O_6$, BSN) with the dielectric permittivity of about 2000-4000. The ITO and BSN films thickness was 0.5 - 1 and 1 - 3 μm respectively. The BSN films are textured with the crystallographic axis C normal to the substrate surface. The crystallites dimensions were 0.3 – 1 μm. The techniques used to obtain the films and their electrophysical properties are described in (Kostsov, 1995; Kostsov & Malinovsky, 1989; Antsigin et al., 1985).

The matrix of the beryllium bronze (2% beryllium) petals with the length l (1 - 4 mm), width b (300-500 μm) and thickness d_p (1.5-2.5 μm) was formed on the moving substrate, see fig.10. This substrate was the optically polished glass plate 0.5 mm in thickness. All the petals had the common electric contact wire (sputtered during the fabrication of the bronze layer) to apply the voltage. The petals became free by etching of the aluminium sacrificial layer from under the petals. To provide for the reciprocal motion, two groups of the petals were created.

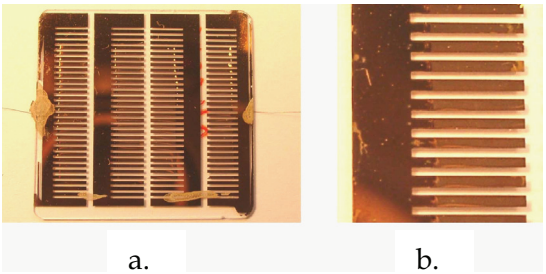


Fig. 10. An example of matrix of the petals design (**a**) and the fragment of the matrix (**b**). Petal size is 0.4*3.5 mm.

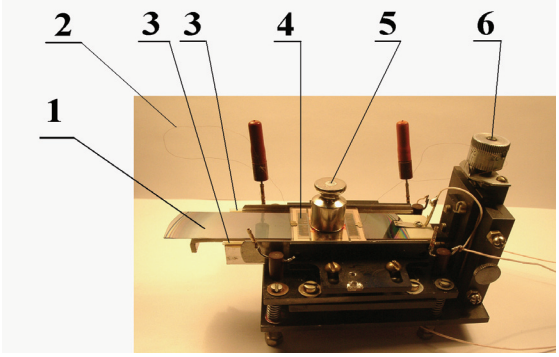


Fig. 11. The experimental set for testing the motor operation. **1** – the bottom substrate (stator), **2** – wires for the contact with the moving substrate, **3** – guides, **4** – moving substrate (slider), **5** – load, **6** – micropositioner for the precise installation of the gap between stator and slider.

The stationary substrate (lower one on the fig.5) and the moving substrate were assembled to form the motor. Two guides were placed between the substrates. For the experiments the probe station was used that allowed one to replace both substrates and adjust the gap between the substrates with good accuracy, see fig. 11.

6. Experimental techniques

To measure the microscopic shift of the slider on the microsecond time scale, the optic technique was developed shown on fig.12. The contrast black-and-white image 2 was attached to slider surface. This image was lit by light beam 6 from laser 7. The image was overlaid with the gap situated in the optical focus of the microscope (lenses 4 and 5) with K-fold zoom. Through the lens 5 the image went to photomultiplier 8. It is easy to show that the electric signal from the photomultiplier will be proportional to the image 2 shift, and the optical resolution of the system will be increased by a factor of K. With K=50 the resolution of about 30 nm was achieved, fig.13.

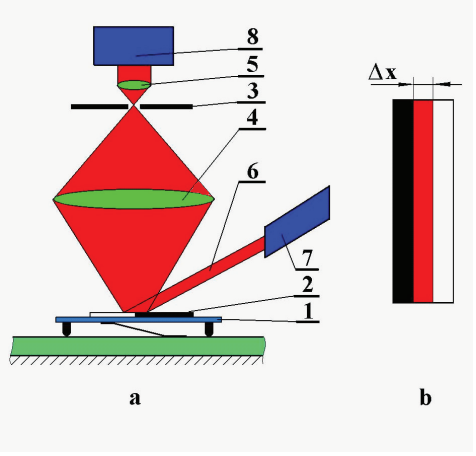


Fig. 12. A method for the optical control of the sample positions. (**a**) is the optical scheme and (**b**) is the image of black and white contrast (**2**), restricted by optical gap (**3**) after the microscop ocular (**5**), Δx is a shadow. **1** – moving plate, **2** – black and white image, **3** – optical gap, **4** – objective lens, **5** – ocular lens, **6** – laser beam, **7** – laser, **8** – photomultiplier.

To separate the components of the total current (capacitance charging current and conduction current) during the electrostatic rolling the integrating technique suggested in (Yun, 1973) was used (see fig.13). The rectangular voltage pulse from the generator 4 was applied to the sample 1 with the time-dependent capacitance C(t) and resistance R(t). The time integral of the current passing through the sample was determined by measuring the potential φ(t) on the measuring capacitor C_m>>C(t), connected in series with the sample 1. Then the signal was amplified (2) and supplied to the analyzer 3 (e.g., oscilloscope). Here

$$\phi(t) = Q(t) / C_m \text{ , where } Q(t) = \int_0^t I(t)dt \text{ -} \tag{12}$$

is the total charge, I(t) – total current, $t<t_p$, where t_p is the voltage pulse duration.

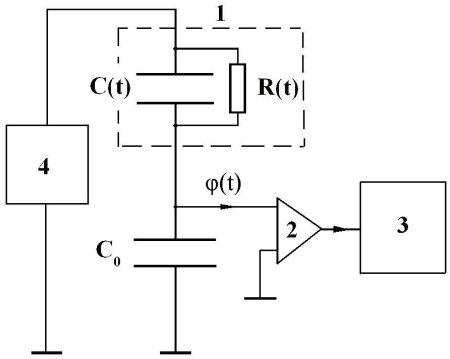


Fig. 13. A schematic representation for the method of capacitance and conductance current separation. **1** – a sample, consisted (schematically) of time-dependent values : C(t) and R(t). $\mathbf{C_0}$ is the measuring capacitance, φ(t) is the measured potential; **2** – amplifier; **3** – oscilloscope; **4** – voltage pulse generator.

Since after the end of the voltage pulse the time Δt necessary to discharge the capacitor C(t) is short and does not depend on the mechanism of the discharge, we have

$$\phi_1(t_p) = \phi(t_p + \Delta t) = \frac{\int_0^{t_p} I_c(t)dt}{C_m} = Q_c(t_p) / C_m \,, \tag{13}$$

where I_c and Q_c are the conductivity current and it's integral, respectively. Then

$$Q_{cap}\left(t_p\right) = \left(\varphi\left(t_p\right) - \varphi_1\left(t_p\right)\right) C_m \quad \text{and} \quad C(t) = Q_{cap}(t) / V, \tag{14}$$

where Q_{cap} is the charge accumulated at the capacitance C(t),V is amplitude of voltage pulse. Thus, by measuring $Q(t_p)$ and $Q_c(t_p)$, it is easy to determine C(t), $I_c(t)$, $I_{cap}(t)$, where $I_{cap}(t)$ is the capacitance charging current. Thus, we separate the conductivity current and capacitance charging current.

The macromotion of the slider was measured using the optical microscope, and the time during which this motion occurred was measured by the number of the voltage pulses and their frequency.

7. Experimental studies of thin-film petal micromotors

The studies conducted with the samples described above, see (Baginsky & Kostsov, 2007), showed that mechanical and electric characteristics qualitatively correspond to the theoretical estimates for the relatively slightly bent petals. In this case the energy conversion efficiency is 60-70% with the rolling time of 1.5-1.7 ms. But relatively low operating frequency (100 Hz and less, see fig.14, curve 3) causes the micromotor to operate with low power. The resonance frequency at which the slider speed reaches maximum corresponds to the resonance frequency f_r of the oscillations of a cantilever with the length l (where l is the petal length):

$$f_r = 0.162 d_p / l^2 (E_Y / \rho)^{1/2}, \quad (17)$$

where d_p is the thickness of the petal, E_Y is the Young modulus, ρ is specific weight. With the petal thickness of about 1.5-2 μm and the Young modulus for berillium bronze $E_Y=10^{11}$ N/m², f_r = 40-60 Hz.

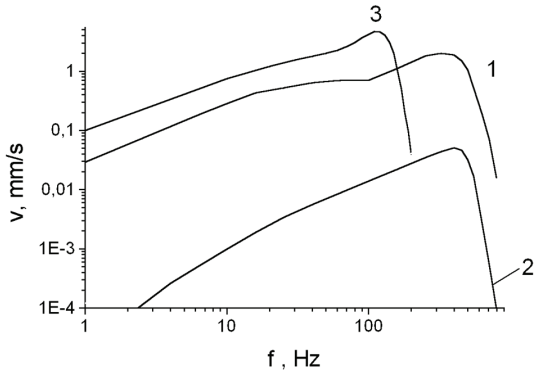


Fig. 14. The frequency dependence of the sample velocity for the cases of bent petals in cross- sectional view (1, 2) and straight petals (3). V=50 V: (1), (3) and V=30 V: (2)

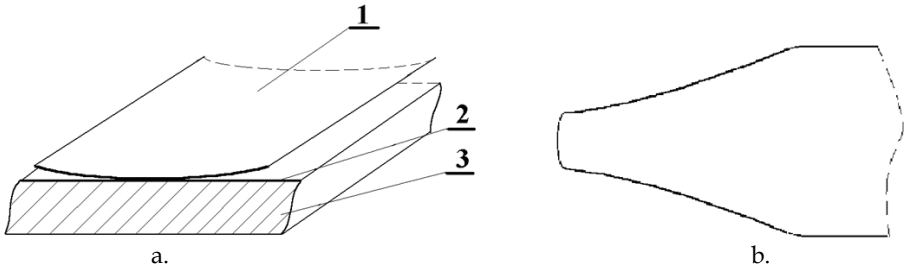


Fig. 15. A view of the bent petal at the position of it's contact with the lower substrate (**a**) and a scheme for the contact surface between the petal and lower substrate (**b**). **1** - petal, **2** – the surface of lower substrate (**3**).

Thus, the most important problem is to increase the clock frequency of the micromotor operation. One of the possible solutions is to use the 3D petals structure, when the radius of curvature of the petal cross-section is comparable to petal width b. The cross-section of this petal (1) at the point of contact with the lower substrate (2) is shown on fig.15a. In this cross-section, the petal acts as a spring with the curvature radius r>b. The lateral cross-section of the petal is straight, with the exception of the contact area with the stator, where the petal is bent (see fig. 5F). During the electrostatic rolling of the petal, this spring is attracted to the ferroelectric surface, and its resonance frequency is determined by its width b, and, if it's length l>>b, is almost independent on length and the applied voltage. It was checked experimentally – the resonance frequency is close to the f_r value obtained when l in equation (17) is replaced with b, see fig. 14, curves 1, 2, in contrast to the straight petals, when the f_r value is determined by their length (curve 3).

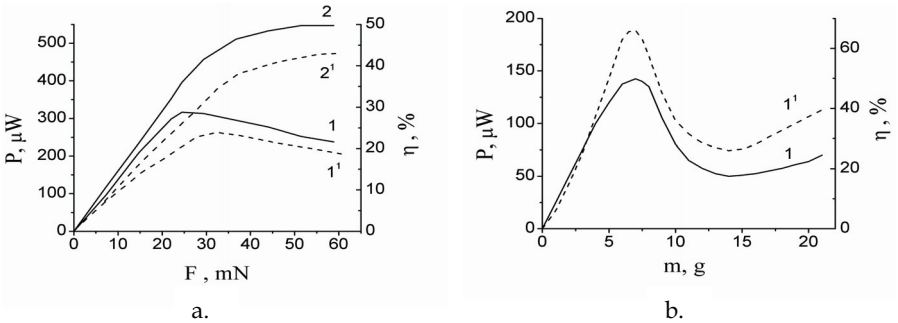


Fig. 16. Power (solid lines) and energy conversion efficiency (dashed lines) as a function of load for the U-shaped (**a**) and flat (**b**) petals with the mass loading (curves (**1**)) and the friction loading (curves (**2**)). The number of petals N=40, f= 1 kHz (**a**), f=100 Hz (**b**).

Moreover the experiments revealed an unusually fast separation of the metallic films (petals) from the ferroelectric surface after the end of the voltage pulse action, discussed above in Sect. 2.

Thus, two factors are identified that can increase the operating frequency of the micromotor. The first one is fast separation of the surfaces; the second one is connected with the 3D petal structure.

The load parameters of the micromotor with 3D petals for the operating frequencies that are close to the optimal ones are shown on figs. 16a and 17. With the mass load, one or more clearly identifiable power peaks were observed, that can be explained by inertia properties (fig.16a, curve 1 and fig.17a, b). The comparison of the load properties of the micromotor for the mass and friction loading, see fig. 16a, have shown that the application of the friction loading should increase power and efficiency (η) of the electromechanical energy conversion. With the friction load, the power was independent on the load value at high enough loads (fig.16a, curve 2). Under these conditions with sufficiently large load, the motor abruptly stopped with further load increase. The power peak (mass load) or plateau (friction load) correspond to switch from the inertial mode to the step mode. In the step mode, the motor comes to stop between the voltage pulses.

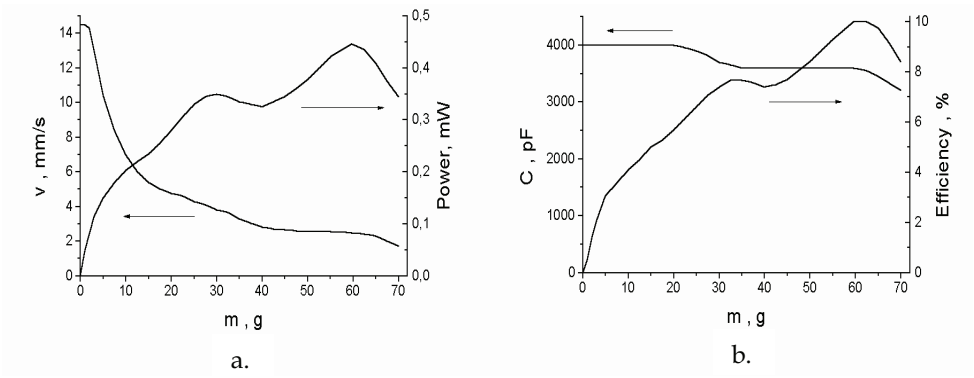


Fig. 17. The multiple peak structure of load characteristics at mass loading.

The relatively low efficiency in the case of U-shaped petal is explained by the fact that in the resonance determined by the petal width only a small part of the petal length comparable to its width participates in the rolling in the stationary periodic mode, and the rest of the petal length spreads along the ferroelectric surface and is periodically attracted to and repelled from it without participating in energy conversion process. So the petal takes the shape of "bulldozer knife".

Higher efficiency can be achieved with the flat petals, but the voltage pulse repetition frequency consistent with the resonance frequency becomes lower, relative pulse duration decreases, and specific power is reduced despite increase in the specific energy, see fig. 16b.

Thus to achieve maximum mechanic power and electromechanical energy conversion efficiency the rolling time must be consistent with pulse repetition frequency. This can be achieved by selection of optimal size and shape of the petals. It can be concluded from the reasoning above that to achieve maximum efficiency the petals must be flat, and to achieve maximum power their length should be decreased. In particular, for operating frequencies on the order of 1 kHz their length should be about 1 mm.

The examples of the slider acceleration as a series of voltage pulses is applied are shown on fig.18 for inertial (a) and step mode (b, c). Here, the pulse length is 0.4 ms, and the pulse repetition rate is 1 ms. In both cases, the slider speed would come to plateau at the second pulse at high energy output (with high V). As V decreases, more pulses are necessary for the complete acceleration, see fig.18a.

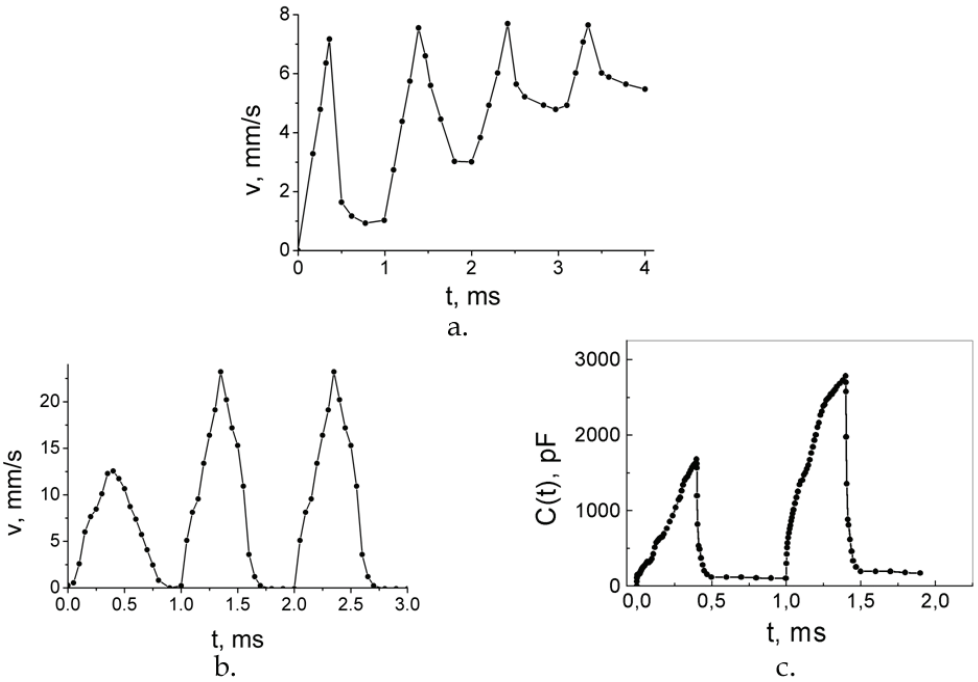


Fig. 18. Slider acceleration in the inertial mode (a) and in the step motion (b). N = 40. (**a)**: M=0.5g, V=40 V, (**b)**: M=5g, V=50 V and (**c**) time variation of the sample capacitance at step mode regime corresponding to Fig.18b (first two steps).

Finally, let's discuss the method of increasing the energy conversion efficiency and power output. Fig. 18b shows the acceleration of the slider in the step mode. The acceleration time depends on the amplitude V. The fact that both power and energy conversion efficiency are higher starting from the second, third, etc. pulse (see fig.18 b, c) means that petals tension increases in the equilibrium step mode. The increase in petal tension can also explain the power increase as the load increases. Thus, after the end of the acceleration stage the efficiency increases and can reach rather high values.

In the equilibrium mode significant fraction of the petals capacitance is not used for the energy conversion, as part of each petal's surface remains parallel to the stator surface because it does not have time to come to the initial state, thus assuming the shape shown on fig. 5c. This shape can be visually observed with the continuous slider motion. On the curves showing C(t) as a function of load this petal shape manifests itself through the large part of the capacitance that is independent on the load value (see fig.17b). Thus, efficiency and power dependences on the load are similar (see fig.16, dotted line corresponds to curve 1-P(F) for the mass load) and fig.17. Significantly more rapid C(t) growth starting from the second, third etc. voltage pulses (see fig.18c) can also be explained by the electrostatic attraction of the part (about 50% according to the estimates) of the petal that did not significantly separate from the ferroelectric surface in the pause between the pulses moving almost parallel to this surface. So when the next voltage pulse is coming this part of the petal is attracting to the ferroelectric surface much more rapidly compared to the first pulse.

The accumulation of the space charge in the ferroelectric leads to the decrease in the efficiency of the energy conversion. This accumulation is connected with both polarization and the injection of the charge carriers under the action of the voltage pulse. After the end of the voltage pulse the electric field still exists on the ferroelectric surface. It attracts the petal and does not allow the petal to assume the initial state. Thus, it interferes with the slider motion in the pause between the voltage pulses. Besides, when the next voltage pulse comes to the ferroelectric surface, the residual potential on the ferroelectric surface when added to the applied voltage decreases the electric field in the metallic film – ferroelectric surface gap. Both these factors lead to deceleration of the slider, and the decrease in the motor power. One of the ways to eliminate the space charge accumulated during the action of the main voltage pulses is the application of the additional pulses (AP) of the opposite polarity in the pauses between the main pulses. Similar processes to alter the potential of the surface at the semiconductor-dielectric boundary with AP are used in the MNOS memory elements (Yun, 1974).

The configuration of the voltage pulses is shown on fig.19d, and the slider speed as function of the additional pulse amplitude V_1 is shown on fig.19a. As the shift between AP and the main pulse grows, its effect on the slider speed increase disappears, see fig.19b. The data shown on fig.19 can be explained by the two phenomena: the compensation of the space charge and the deceleration of the slider due to the application of voltage pulse V_1, even if for a short time. When AP is applied right after the main pulse, the deceleration plays positive role, leading to the separation of some part of the petals from BSN surface even with applied AP. The latter effect manifests itself through the decrease in the capacitance C some time t after the start of AP (see fig.19c). The following AP parameters were chosen experimentally: amplitude V_1= -17 V, duration t_1 = 50 μs. With these AP parameters the speed of the slider and the micromotor power are by a factor of 1.5- 2 higher as compared with the mode when AP is not used.

The main reason for the decrease in the energy conversion efficiency as the petal assumes the form shown on fig.5C, which excludes part of the petal from the energy conversion process is the mismatch between the frequency corresponding to the motor's maximum power and the natural frequency of the petal's vibrations. For example, for the petals

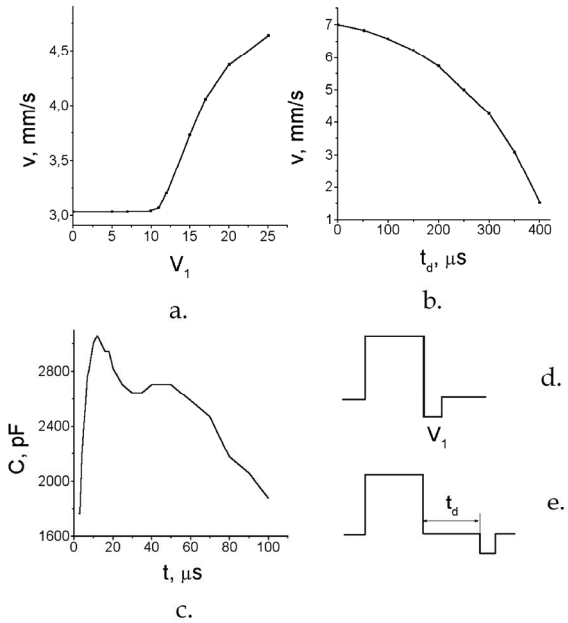


Fig. 19. The characteristics of the motor behavior under conditions, when additional voltage pulse (AP) is applied. **a** – the dependence of slider velocity on the amplitude of AP – V_1 (configuration **d**), **b** - the dependence of slider velocity on the delay between main and additional pulses – τ_d (configuration **e**), **c** – the dependence of the structure capacitance on the AP duration.

shape shown on fig. 15a with the operation frequency of 1 kHz, the on-line time ratio of the pulses was 0.5, yet the efficiency was less than 20-25%, because the resonance of that frequency corresponded to petal's width. In case of flat petals, the efficiency was 70-80%, but the operating frequency decreased to 100-40 Hz, which resulted in the on-line time ratio increase by a factor of 10-20. Thus, despite the increase in the mechanical energy generated during one conversion cycle by a factor of 3-4, the power was fallen down by a factor of 3-5

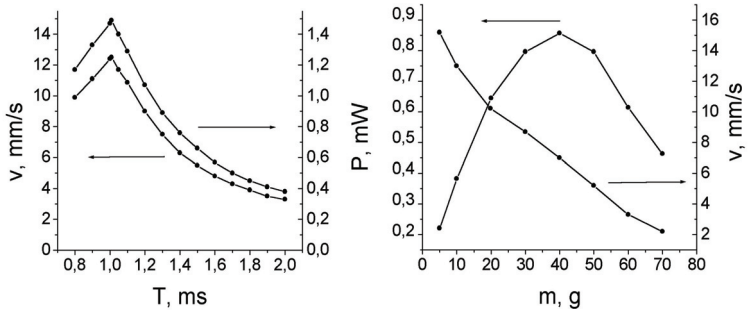
The second reason for the incomplete conversion of the rolling capacitance energy into the mechanical energy is the incomplete rolling of the petal's surface, that is, the formation of the so called rolling needle shown on fig.15b. The formation of this needle can be attributed to the difference in the speed v_l of the longitudinal (along the petal's length) rolling and speed v_b of the lateral rolling, because initially the petal has the 3D structure shown on fig.15a. This results in the motive force decrease, because in this case only the part of the petal's width that is on the front end of the rolling contributes to the driving force (see fig.15b). It can be noted that this phenomenon can explain the possibility of the significant efficiency increase with the practically unchanged power by increase in the petal's stiffness achieved by small increase in the thickness. In this case the efficiency increase with the rolling capacitance decrease can be attributed to the decrease in the unused capacitance. This happens because relatively smaller part of the lateral surface of the petal is rolled because of the increase in the lateral stiffness. The above mechanism can explain steep

(faster than quadratic) growth of P as a function of V at the low voltages. At high voltages, P is quadratic function of V, because the growth in voltage increases the lateral rolling speed and leads to the rolling needle disappearance.
The decrease in the petal length accompanied by appropriate (roughly proportional) decrease in the gap thickness d_e allows one to achieve the resonance motion of the slider with respect to the petal length, and thus achieve high efficiency accompanied by the specific power increase. To increase power by an order of magnitude it is necessary to use 0.5 mm and shorter petals.

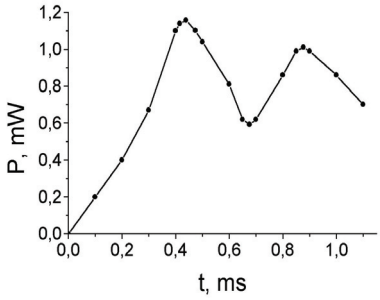
8. The peculiarities of ferroelectric ceramic application in petal micromotors

To create micromotor prototype thin ceramic plates were used made of PZT material with the composition Pb0 - 66%, ZrO_2 - 21%, TiO_2 - 11% and dielectric constant of $\varepsilon_F \sim 3900$. Also, we used plates made of antiferroelectric ceramics with the composition close to PZT and dielectric constant of 10000. The surfaces of the ceramic plates used for the electrostatic rolling were polished up to the optical smoothness (roughness of about 10^{-8} m). The metallic electrode (silver film with 1 μm thickness) was applied to another ceramic surface by vacuum deposition followed by sintering.
One of the peculiarities arising from the use of the ferroelectric ceramics in the described construction, as opposed to the use of barium-strontium niobate films (Dyatlov et al., 2000; Baginsky & Kostsov, 2003) is higher value of the switched polarization part and longer time before polarization disappearance.
To significantly decrease the effect of the polarization switch in the step mode, it is necessary to apply the pulse of the opposite polarity with length and amplitude sufficient to bring the polarization direction into its initial state before the application of the slider moving pulse. But even this scheme of voltage pulse application does not completely solve the problem of polarization screening charge, since between the pulses there is an electric field near the ferroelectric surface that causes the slider to stop and decreases the motor power.
The investigations of micromotors made on the basis of PZT ceramics revealed only a small values of mechanical energy and specific power because of high values of polarization damping the motion.
The effect of the polarization processes can be significantly decreased by using antiferroelectric materials with high ε, that are shown to have quite small or no residual polarization (Burfoot & Taylor, 1979).
The ceramics was 100 μm thick, with the specific capacitance of about 900 pF/mm². The specific capacitance during the electrostatic rolling was only 20 – 40 % smaller than that of the ferroelectric films despite higher thickness. Since the use of AFE ceramics allows one to apply significantly stronger voltage pulses than would be possible for the ferroelectric films without compromising the operation reliability, it is obvious that the energy capacitance and motor power can also be significantly increased.
Fig. 20 shows the frequency (a) and load (b) properties of the micromotors based on the AFE ceramics for the constant number (n=40) and size (3.5*0.5mm) of petals and their dependence on the voltage pulse duration (c). To eliminate the effect of the space charge that is created by the leakage current caused by the voltage pulse, after the end of the main pulse (MP) the additional pulse (AP) was applied with the amplitude equal to that of the MP, but of the opposite polarity and with smaller duration (100 μs). This relationship between MP and AP parameters was found experimentally to maximize the power of the micromotor with the given load.

The analysis of the frequency properties of the motor power (fig. 20a) showed the resonance at clock frequency of about 1 kHz. The resonance position was virtually independent on voltage pulse amplitude and motor power and load. It shows that the peak can be mainly attributed to the mechanical resonance based on the petal width.
For the fixed load and voltage pulse amplitude the micromotor power can be maximized by adjusting the pulse duration and the time between the pulses. For example, fig.20c shows the typical curve of micromotor power as a function of pulse duration, with the optimal pulse duration of 450 μs. The complex shape of this curve with two maximums is explained by manifestation of two effects. The first peak appears due to the mechanical resonance of the petal at frequency of about 1 kHz (Baginsky & Kostsov, 2003). As the pulse duration t_p grows at the conditions of fixed gap between the pulses Δt the additional part of the petal's length is involved in the process. It gives rise to the additional grows of power despite of the frequency $f = 1/T$ (where $T = t_p + \Delta t$) decrease, so the second peak is forming.
Load curves, fig. 20b show the power peak at 40 g load (the friction coefficient k is 0.3). The maximal power was 1.5 mW, which is 2-3 times greater than for the similar motor based on the ferroelectric films.



a. b.



c.

Fig. 20. Power and speed of the antiferroelectric ceramics motor, (**a**) – as a function of voltage pulse period (m = 40 g, t_p = 0.45 ms), (**b**) – of the load mass (T = 1 ms, t_p = 0.4 ms) and (**c**) - of the voltage pulse duration. m = 40 g, V = 85 V, t_1 = 0.1 ms.

Table 1 compares the maximal absolute and specific power, P and P_1, with the same mass load, friction coefficient (k=0.3) and number of petals (n=40) for motors based on barium-strontium niobate (BSN) films ($Ba_{0.5}Sr_{0.5}Nb_2O_5$ composition), PZT-ceramics and AFE-ceramics.

Material	P, μW	Petal size, mm	P_1, μW/mm²	V, volts
BSN films	500	3.5*0.5	7.14	50
PZT-ceramics	70	3.5*0.5	0.83	90
AFE- ceramics	1500	3.5*0.5	21.4	85

Table 1. A comparison of power of petal electrostatic micromotors on different materials.

Micromotor power can be increased by decreasing d down to 50-20 μm, or by increasing voltage pulse amplitude up to the breakdown voltage in the gap between the petal and the ferroelectric surface. According to estimates in (Dyatlov, et. al., 1996), this voltage can be as high as 200 V.

Besides, the power of the linear motor can be increased by increasing the operation clock frequency, the optimal value of which in turn depends on resonant frequency of the petal as have been shown above.

Thus the duration of the separation process does not affect the frequency properties of the motor, and clock frequency is limited by the duration of the electrostatic rolling process. The experimental clock frequencies for the ferroelectric films are in 10 – 20 kHz range (Dyatlov et al., 2000). Thus, the maximum specific power of the "ceramic" motor can be estimated to be equal to 100 – 300 μW/mm².

9. Some applications of the micromotors

High energy output allows one to obtain high absolute power (up to 0.01 – 1 W) increasing the rolling area, and therefore the described micromotors can be used in various MEMS devices, e.g., listed in Introduction.

Some applications of proposed micromotors in MEMS were analyzed by us both numerically and experimentally.

The possibility of creation of high speed (microsecond range) microcommutators powered by microactuator based on an electrostatic rolling of the thin metallic film on the ferroelectric film surface was considered in (Kostsov & Kolesnikov, 2007). The numerical analysis of the microcommutator operation was performed and its main characteristics were described. It was shown that the driving force developed by the microactuator in the first 10–100 μs of the electrostatic rolling is equal to 0.05–0.5 N per 1 mm of metallic film width, and the force is limited by the mechanical strength of the film. The high value of the force makes it possible to use strong springs that prevent the switchboard from switching between steady states even under the load factor of 1000 g and more

The research on opportunities of construction of high – efficiency micropumps and injectors of liquid microjets on the base of high energy-intensive electrostatic microactuators, working in a cyclic mode, was carried out (Kostsov & Sokolov, 2010). The design, the features of functioning, characteristic parameters of such devices are described. It is shown that a microactuator with the area of 1 mm² is capable to inject during one step with the duration of 30-300 μs a microjet of liquid with the weight of 1 - 3 micrograms, flowing out with the velocity of 1-10 m/s and more depending on the radius of exit nozzle.

Electrostatic high energy micromotor based on the ferroelectric films is studied as applied to microelectromechanical devices operating in vibrational mode (Baginsky et al., 2008). It is shown that the micromotor can be efficiently used in high frequency micromechanical vibrators that are used in high energy MEMS devices, such as micropumps, microvalves, microinjectors, adaptive microoptic devices etc.

The operation principle of micromechanical valve based on the effect of electrostatic rolling of metallic films on the ferroelectric surface was considered (Kostsov & Kamishlov, 2006). These microvalves differ from prototypes by high operation speed (microseconds), by ability to sustain a high pressures and by good fabricability.
Finally, the preliminary experiments and numerical modelling have shown that these microactuators can be used as microelectrogenerators with wide application range by reversing the described electromechanical energy conversion (Baginsky & Kostsov, 2002).

10. Results and discussion

The comparison of the operation parameters for the different types of the electrostatic micromotors is shown in table 2. Here $A_R = C_{sp}V^2/2$ is the electric work during one cycle. Mechanical work is $A_M = \eta A_R$. The energy conversion efficiency η value is determined by the micromotor construction. For the first two types of the micromotors relatively high efficiency values are achieved – up to 80%, for the micromotor described in this paper the efficiency can also be as high as 80% depending on the petal geometry. The analysis of the data in Table 2 shows the specific mechanical work of the described micromotors to be greater than A_M values typical for the known constructions of the micromotors used in MEMS by several orders of magnitude.

Micromotor type	d, μm	C_1, pF/mm²	V, Volts	A_R max. J/m²	A_R V=50 V J/m²	A_M V=50 V J/m²	A_M max. J/m²
Air gap	2-3	<4	0-50	10^{-2}	$5\ 10^{-3}$	$4\ 10^{-3}$	10^{-3}
Rolling on the linear dielectric	2-3	40	0-150	$5\ 10^{-2}$ –0.5	$5\ 10^{-2}$	$4\ 10^{-2}$	$4\ 10^{-1}$
Rolling on the ferroelectric	2-3	300-1000	20-200	5	1.3	1.05	1.25

Table 2. Comparison of the parameters of the different types of the electrostatic micromotors

This work shows that high energy output step reversible micromotors based on the ferroelectric layers can be created by micromachining for use in such MEMS where high specific power and operation speed are necessary.
These micromotors have the following advantages compared to the classical piezoelectric motors utilizing converse piezoelectric effect:

- higher unit step: 10 –20 μm per 1 mm of petal length rather than 1 μm per 1mm of ceramics length,
- longer range of slider motion: it is essentially equal to the length of the ferroelectric layer,
- microelectronic design and manufacturing,
- higher specific energy output (up to 100 W/kg) and driving force (up to 10^3- 10^4 N/kg),
- lower operating voltage necessary for the motion start,
- significantly lower hysteresis,
- flexible movement control, including reversible movement.

Studies of the reliability of the elements based on the bending effects in thin freely suspended films (which are used, for example, to form elements of dynamic diffraction gratings) showed that they have a high reliability, allowing for up to 5×10^{12} bending cycles without a significant change in the parameters (Trisnadi, 2004). The fatigue properties of bronze films have been well studied; their distinctive feature is the ability to withstand long-

term cyclic loads (more than 10^{12} cycles), provided that the sum of bending and tension stresses does not exceed the limiting fatigue stress (400—600 N/mm^2). In the problem under consideration, the electric strength of the ferroelectric film would not reduce the reliability of elements containing this film, because only a small part of the applied voltage drops on it. These micromotors can be used in MEMS devices in the following areas: step micro- and nanopositioners (one and two-dimensional), microoptics, adaptive optics, high-speed lightguide switches, microscanners, micropumps, e.g. for the inkjet cartridges, indicators, indicator panels, sensors, control and diagnostic systems, microgenerators of electric power, etc.

High energy output allows one to obtain high absolute power (up to 0.01 – 1 W) increasing the rolling area, and therefore the described micromotors can be used in macroscopic devices such as microair vehicles, microrobots, artificial muscles etc.

11. References

Akiyama T. & Fujita H. (1995). A quantitative analysis of scratch drive actuator using buckling motion. *Proceedings of Micro Electro Mechanical Systems, 1995, MEMS'95.IEEE,* pp.310-315. ISBN 0-7803-2503-6, Amsterdam, the Netherlands, 29 January-2 February 1995.

Antsigin V. D., Egorov V. M., Kostsov E. G. & Sterelychina L. N. (1985) Ferroelectric properties of thin strontium barium niobate films. *Ferroelectrics,* Vol. 63, No. 1, pp. 235-242, ISSN 0015-0193.

Baginsky I., Kostsov E. & Sobolev V. (2008). High energy microelecromechanical oscillator based on the electrostatic microactuator. Proc. SPIE, Vol. 7025, pp. E1-E8, ISSN 0277-786X.

Baginsky I.L. & Kostsov E.G. (2002). The possibility of creating a microelectronic electrostatic energy generator. *Optoelectronics, Instrumentation and Data Processing (Avtometriya.),* No.1, pp.89-102, ISSN 8756-6990.

Baginsky I.L. & Kostsov E.G. (2003). High-energy capacitance electrostatic micromotors. *J. Micromech. Microeng*., Vol. 13, No. 2 , pp. 190 – 200, ISSN 0960-1317.

Baginsky I.L. & Kostsov E.G. (2004). Electrostatic micromotor based on ferroelectric ceramics. .J. Micromech. Microeng., Vol.14, No.11, pp. 1569- 1575, ISSN 0960-1317.

Baginsky I.L.& Kostsov E.G. (2007). High energy-density MEMS based on thin ferroelectric layers. *Ferroelectrics*, Vol. 351, No.1, pp. 69-78, ISSN 0015-0193.

Baginsky I.L.& Kostsov E.G. (2010). Reversible high-peed electrostatic "contact". *Semiconductors,* Vol. 44, No. 13, pp. 1654-1657. ISSN 1063-7826.

Burfoot J.C., & Taylor G.W. (1979). *Polar Dielectrics and Their Applications.* The Macmillian Press LTD, ISBN 0-520-03749-9, London – New Jersey.

Dyatlov V. L. & Kostsov E. G. (1998) Electromechanical energy converters of micromechanic devices on the basis of ferroelectric films. *Nuclear Inst. and Methods in Physics Research,* Vol. A 405 No. 2-3, pp. 511-513, ISSN 0168-9002.

Dyatlov V. L. & Kostsov E. G. (1999). High–effective electrostatic micromotors on the basis thin ferroelectric films. *Optoelectronics, Instrumentation and Data Processing (Avtometriya.),* No.3, pp 3-15, ISSN 8756-6990.

Dyatlov V. L., Kostsov E. G. & Baginsky I. L. (2000). High-effective electromechanical energy conversion on the basis of thin ferroelectric films. *Ferroelectrics* , Vol. 241, No.1, pp. 99 – 106, ISSN 0015-0193.

Dyatlov V.L, Konyashkin V.V., Potapov B.S. & Pyankov Yu.A. (1996). Planar electrostatic micromotors. *Electrical Technology* (Elsevier Sequoia), No. 1, pp. 1 – 18, ISSN 1028 – 7957.

Dyatlov V.L., Konyashkin V.V., Potapov B.S. & Pyankov Yu.A. (1991). *Film Electrostatics.* Nauka, ISBN 5-02-029683-X, Novosibirsk (in Russian).

Esashi M. & Ono T. (2005). From MEMS to nanomachine. *J. Phys. D: Appl. Phys,* Vol. 38, No. 13, pp.R223–R230, ISSN 0022-3727.

Harness T. & Syms R. R. A. (2000). Characteristic modes of electrostatic comb-drive X-Y microactuators. *J. Micromech. Microeng.,* Vol. 10, No. 1, pp. 7–14, ISSN 0960-1317.

Kim B.-H. & Chun K. (2001). Fabrication of an electrostatic track-following micro actuator for hard disk drives using SOI wafer. *J. Micromech. Microeng.,* Vol. 11, No. 1, pp.1–6, ISSN 0960-1317.

Kostsov E.G. & Kamishlov V.F. (2006). Microelectromechanical Micro-Valve. *J. nano and microsys. techn.*, N 12, pp. 57 -59, ISSN 1813-8586.

Kostsov E.G. & Kolesnikov A.A. (2007). Fast electrostatic microcommutators based on the ferroelectric films. *Ferroelectrics*, Vol. 351, No. 1, pp. 138-144, ISSN 0015-0193.

Kostsov E.G. & Malinovsky V.K. (1989). Large-scale use of ferroelectricity in microelectronics is reality. *Ferroelectrics,* Vol. 94, No. 4, pp. 457-462, ISSN 0015-0193.

Kostsov E.G. & Sokolov A.A. (2010). Microelectromechanical fuel injector for diesel engines. *Journal of nano and microsystem technique*, No 8, pp. 30 – 34, ISSN 1813-8586.

Kostsov E.G. (1995). Ferroelectric films: peculiarities in their application to construction of new generation of memory devices. *Ferroelectrics,* Vol. 167, No. 3-4, pp. 169-176, ISSN 0015-0193.

Kostsov E.G. (2005). Ferroelectric barium-strontium niobate films and multi-layer structures. *Ferroelectrics*, Vol. 314, No. 1, pp. 169-187, ISSN 0015-0193.

Kostsov E.G. (2008). Electromechanical energy conversion in the nanometer gaps. *Proc. of SPIE*, Vol. 7025, pp. G1-G8, ISSN 0277-786X.

Kostsov E.G. (2009). Status and prospects of micro- and nanoelectromechanics. *Optoelectronics, Instrumentation and Data Processing*, Vol. 45, No. 3, pp.189- 226,. ISSN 8756-6990.

Sato K. & Shikida M. (1992). Electrostatic film actuator with a large vertical displacement. *Proceedings of Micro Electro Mechanical Systems, 1992. MEMS'92. An Investigation of Micro Structures, Sensors, Actuators, Machines and Robot.IEEE,* ISBN 0-7803-0497-7, Travemunde , Germany, 4-7 February, 1992, pp. 1-5,.

Trisnadi J.I., Clinton B.C. & Monteverde R. Overview and applications of Grating Light Valve™ based optical write engines for high-speed digital imaging. (2004). *Proc. SPIE,* Vol. 5348, pp. 52-54, ISSN 0277-786X.

Wallrabe U., Bley P., Krevet B., Menz W. & Mohr J. (1994). Design rules and test of electrostatic micrimotors made by the LIGA process. *J. Micromech. Microeng.,* Vol. 4, No. 4, pp. 40–45, ISSN 0960-1317.

Yun B. H. (1973). Direct display of electron back tunneling in MNOS memory capacitor. *Appl.Phys.Lett.,* Vol. 23, No. 3, pp.152-153, ISSN 2158-3226.

Yun B. H. (1974). Measurements of charge propagation in Si_3N_4 films. *Appl. Phys. Lett.,* Vol. 25, No. 6, pp. 340- 342, 2158-3226.

Zappe S., Baltzer M., Kraus T. & Obermeler E. (1997). Electrostatically driven micro – actuators: FE analysis and fabrication. *J. Micromech. Microeng.,* Vol. 7, No. 3, pp.204-209, ISSN 0960-1317.

3

Periodically Poled Acoustic Wave-Guide and Transducers for Radio-Frequency Applications

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1. Introduction

The demand for highly coupled high quality acoustic wave devices for RF signal processing based on passive devices has generated a strong innovative activity, yielding the investigation of new excitation principles and waveguide structures. Among all the tested devices, one can mention thick passivation SiO_2-based structures using high velocity modes on lithium niobate ($LiNbO_3$) or lithium tantalate ($LiTaO_3$) (Kando et al, 2006), (Gachon et al. 2010), yielding the definition of interface or isolated-wave-based devices but modes excited on compound substrates (Elmazria et al, 2009), for instance consisting of a piezoelectric layer (AlN, ZnO, single crystal $LiNbO_3$ or $LiTaO_3$, etc.) deposited atop a high acoustic wave velocity material such as diamond-C, silicon carbide, sapphire, silicon, and so on (Higaki et al, 1997), (Iriarte et al, 2003), (Salut & al, 2010). All these devices generally exploit inter-digitized transducers (IDTs) operating at Bragg frequency (Morgan, 1985), i.e. exhibiting a mechanical period equal to a half-wavelength of the acoustic propagation. Although passivation allows for an improved power handling compared to IDTS on free surfaces, this feature is still limited by electro-migration and material diffusion phenomena (Greer et al, 1990). An interesting answer to this problem is the use of bulk acoustic waves in thin films exhibiting a high disruptive field material such as AlN (Lakin, 2003), (Lanz, 2005). In that case, the frequency control reveals more difficult than for IDT based devices, as the resonance frequency of the so-called Film Bulk Acoustic Resonators (FBARs) is proportional to the film thickness. As significant progresses were achieved in thin film technologies during the last decade, this did not prevent the use of FBARs for actual low-loss RF filter implementation (Bradley et al, 2000). Nevertheless, it turns out there is still missing capabilities for better controlling the operation frequency of these passive devices, particularly for future generations of telecommunication systems which push toward higher RF bands than those exploited until now.

The idea to transfer the transducer periodicity within the substrate has been shared by numerous scientists but it took rather a long term before the first experimental evidence, allowing for a correlation between theory and experiment and hence yielding a satisfying explanation of the corresponding mode distribution and realistic property description.

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Although our very first proof of concept were built on a PZT substrate (Ballandras et al 2003) and after on an epitaxial PZT thin film grown on $SrTiO_3$ (Sarin Kumar et al, 2004), the first convincing experiments were performed on 500µm thick 3" $LiNbO_3$ Z-cut wafers of optical quality answering severe specifications on total thickness variation and side parallelism (Courjon et al, 2007). The fabrication of periodically poled transducers (PPTs) on such wafers has allowed for the excitation of symmetrical Lamb modes with an operating frequency twice higher than those obtained using standard inter-digitized transducers. The corresponding devices have been successfully manufactured and tested, the measured electrical admittances perfectly agreeing with theoretical predictions. As in the case of classical Lamb waves, the fundamental mode was found almost insensitive to the wafer thickness. The frequency control then is achieved by the poling period, whereas the excitation principle coincides with the one of FBARs and hence allows for improved power handling capabilities regarding standard SAW transducers.
These experiments were followed by the fabrication of PPT-based wave-guides. One more time, technology advances allowing for room-temperature reliable bonding of heterogeneous material based on metal-metal compression and lapping/polishing operations (Gachon et al, 2008), PPTs built on single crystal $LiNbO_3$ Z-cut layers were bounded atop Silicon and lapped down to a few tens of µm to develop RF passive devices compatible with silicon-based technologies (Courjon et al, 2008). Once again, a good agreement between theory and experiments was emphasized. Two main contributions to the electrical admittance of the test devices were identified as an elliptical mode and a longitudinal propagation radiating in the substrate. The first mode was found again low sensitive to the $LiNbO_3$ thickness and the technological achievement proved the feasibility of thinned-$LiNbO_3$-layer-based PPT/Silicon devices.
These results were sufficiently convincing for pushing ahead the investigations toward even more complicated structures. An innovative solution then was proposed to address' the need for spectral purity, immunity to parasites, simple packaging and fabrication robustness (Bassignot et al, 2011). The proposed structure is still based on PPT but the later is inserted between two guiding substrates. It was pointed out first theoretically and afterward experimentally that a wave could propagate without any acoustic losses and decreases exponentially in such a structure (definition of a guided mode). This description is close to the one of interface waves (Kando et al, 2006) and fairly coincides with the behavior of isolated wave (Elmazria et al, 2009). In the proposed approach however, two metal-metal bonding are required and naturally provide the excitation electrodes, yielding a significant simplification of the device fabrication compared to classical IDT-based devices. One more time, theory and experiments were according well, and the implementation of such a waveguide for the fabrication of a one-port resonator has been demonstrated (Bassignot et al, 2011). This resonator was used to stabilize a Colpitts oscillator, allowing for stability measurements. Another convincing application was demonstrated by Murata (Kadota et al, 2009) for a RF filter operating at a quite low frequency but exhibiting a double mode transfer function yielding sharp transition bands, a rejection of about 20 dB with small insertion losses (less than 5 dB). Although not accurately explained in the above-referred text, one can actually guess that the filter operation is based on mode coupling as the filter architecture does not leave any possibility for other operation principles.
In this chapter, some fundamental elements are reported to understand the transducer operation. Theoretical analysis results and theory/experiment assessments are shown, allowing to illustrate the level of control for designing actual devices based on that principle. Technological aspects concerning the poling operations as well as bonding and

lapping/polishing techniques are briefly reminded. The fabrication and test of more complicated waveguides are then described and finally the use of Si/PPT/Si resonators for oscillator purposes is presented. As a conclusion, further developments needed to widen to more applications (such as filters or even sensors) are discussed, pointing out the advantages of the principle but also the points for each more investigations are still needed.

2. Basic principle of PPTs

The Periodically Poled Transducer is fundamentally based on a periodically poled piezoelectric medium (see Fig.1). Each side of this medium is metalized in order to obtain a capacitive dipole in which elastic waves can be excited by phase construction. Such a periodically poled structure can be advantageously achieved on ferroelectric materials like PZT thanks to the rather small value of its coercive electric field (the absolute value of the electric field above which the spontaneous polarization can be inverted) or $LiNbO_3$ and $LiTaO_3$. It advantageously compares to standard surface acoustic wave (SAW) devices considering its natural operation, yielding a factor of two for the working frequency as it exploits a second harmonic condition (contrarily to SAW which operates at Bragg frequency). Also it exhibits an advantage compared to film bulk acoustic resonator (FBAR) as the periodicity controls the operation frequency (and not only the plate thickness as for FBAR).
As mentioned in introduction, the first mode of most PPT-based device is low sensitive to the ferroelectrics plate thickness and therefore the solution reveals more robust than bulk wave devices considering frequency control. An intuitive analysis of the device operation yields the conclusion that only symmetrical modes can be excited in plates exhibiting geometrical symmetry. This consideration of course fails as soon as the PPT is bonded on a substrate, but it still holds for Si/PPT/Si structure.

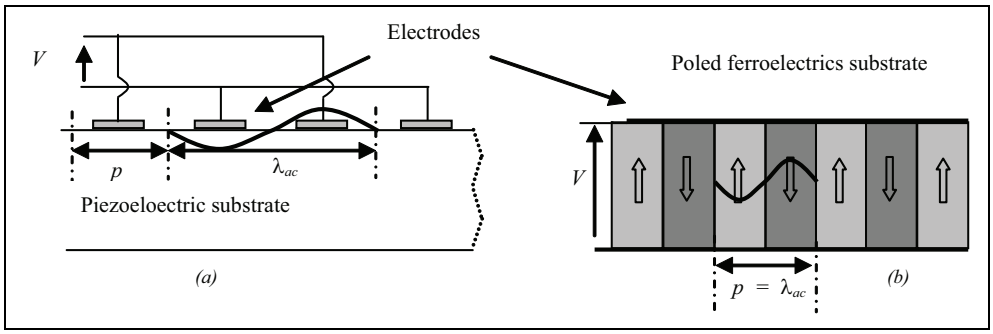


Fig. 1. Comparison between principles of standard SAW devices (a) and poled ferroelectric film transducers (b)

Whatever, the simulation of PPT cannot be achieved using simple harmonic models or even Green's function analysis. Even if analytical efforts have been initially achieved to predict PPT efficiency, the use of finite element analysis has revealed particularly advantageous and much more flexible than plane-wave expansion approaches for instance (Wilm et al, 2002). Furthermore, for estimating guiding capabilities of PPT bonded on substrates, the combination of finite element and boundary element achieved for passivated SAW devices (Ballandras et al, 2009) or interface waves (Gachon et al, 2010) is ideally suited.

3. Technological developments

3.1 Periodic poling of ferroelectrics single crystal

As mentioned above, the poling process can be rather easily applied to PZT for which the coercitive field is small enough to allow for an efficient control of the domain polarity. In the case of lithium niobate or tantalate, this situation is quite different because of the large value of their coercitive fields (21 $MV.m^{-1}$ compared to 2.5 $MV.m^{-1}$ max. for PZT). As a consequence, the development of a dedicated poling bench was required to control the poling of thick (500µm) Z-cut $LiNbO_3$ and $LiTaO_3$ plates. This is detailed in ref (Courjon et al, 2007). Consequently, only a brief description of the bench principle is reported here. The poling bench mainly consists of a high voltage amplifier used to submit the ferroelectrics wafer to an electric field strong enough to invert its native polarization. To achieve such an operation, one needs the use of optical grade Z-cut plates. Wafers are cut in the same boule to well control the poling conditions. A photoresist mask is achieved atop one wafer surface, which defines the poling location. A lithium chloride electrolyte is used to ensure good electric contacts with the wafer surfaces. A dynamic poling sequence then is imposed to the wafer, progressively reaching the expected coercitive field. An evidence of successful poling is obtained by measuring the current of the whole electrical system. Once evidence of transient current obtained, the device is considered to be poled. Following this sequence, and providing no short circuit occurs, an almost perfect poling can be achieved. Figure 2 shows a principle scheme of the poling bench.

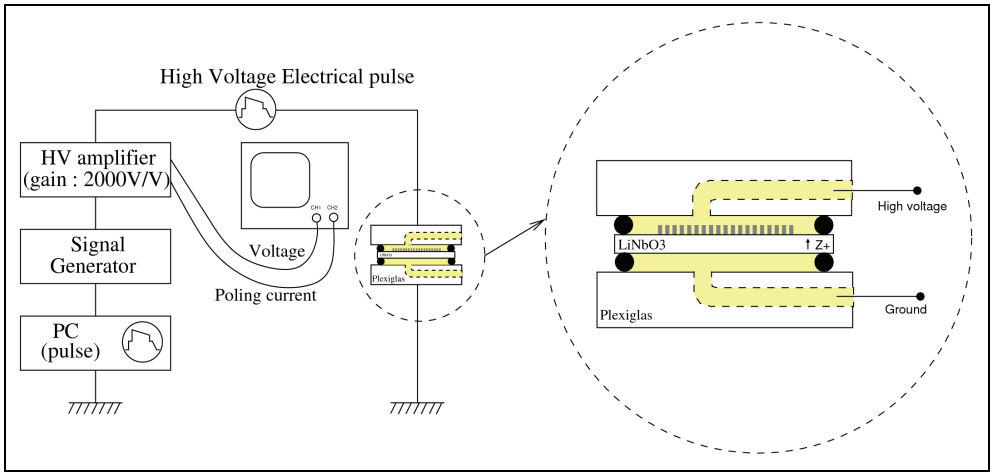
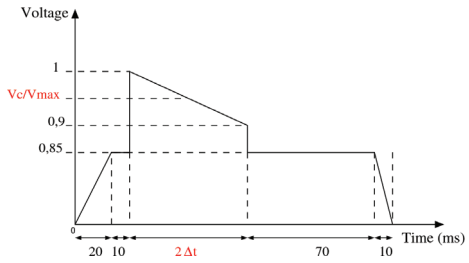


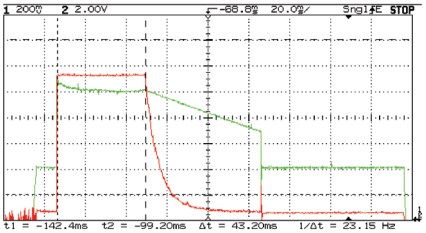
Fig. 2. Scheme of the poling bench used to fabricate periodically poled ferroelectric plates

Our experiments have been achieved on thick (500 µm) optical quality Z-cut $LiNbO_3$ plates from CTI (CA, USA) and on Z-cut LiTaO3 plates from Redoptronics (CA, USA). Consequently, the voltage needed to invert the domains is approximately 11kV. The domains to be poled have been defined using a photo-resist pattern on one plate surface with poling periods (i.e. acoustic wavelengths) ranging from 50 to 5 µm (corresponding to 2.5 and 25 µm line-width respectively). The plate is held in a plexiglas (PMMA) mounting by means of two O-ring which create two cavities fulfilled by the saturated lithium chloride solution used as a liquid electrode (as it is shown in the scheme of fig.2).

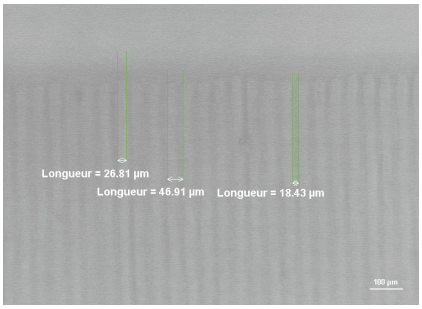
The high poling voltage is applied to the plate following the sequence established by Myers et al. (Myers et al, 1995). This sequence is designed to favor the domain nucleation, to stabilize the inverted domains (i.e. to avoid back-switching of the domains) and to avoid electrical breakdowns. The poling process is monitored by measuring the electric current crossing the wafer during the sequence. The signature of a successful domain inversion corresponds to a voltage dropping, due to the high voltage amplifier saturation, while a current discharge occurs simultaneously. The poling can be easily controlled by a simple optical post-observation, as it generates a contrast between at the edge of the poled domains. We have emphasized that although the $LiNbO_3$ poling was quicker and simpler than the $LiTaO_3$ one, the later was more controllable once increasing the stabilization delay. Figs 3 & 4 show normalized electrical pulse and example of successful poling for both materials.



(a)



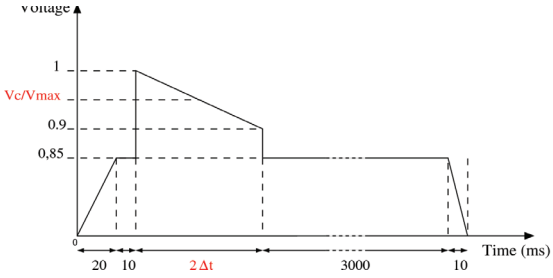
(b)



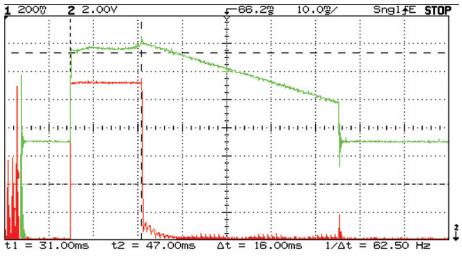
(c)

Fig. 3. (a) Normalized electrical pulse for the $LiNbO_3$ poling, (b) Electrical potential (green) and current (red) provided by the amplifier to the poling circuit (c) Optical microscope observation of a periodically poled lithium niobate substrate

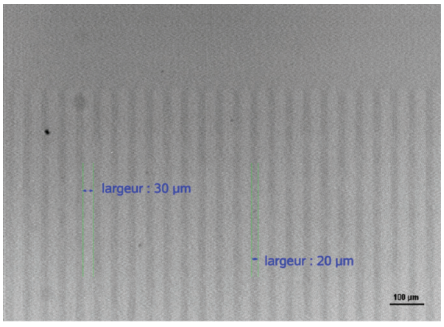
We have tested various configurations of Lamb-wave PPTs, the simplest configuration using the periodic poling approach just consisting in depositing electrodes on both side of the poled plate. Both practical implementation and simulations have been developed, based on the above-described approach and on finite element analysis for the later. Figure 5 shows that an excellent control of such device and an accurate description of its operation can be achieved.



(a)



(b)



(c)

Fig. 4. (a) Normalized electrical pulse for the $LiTaO_3$ poling, (a) Electrical potential (green) and current (red) provided by the amplifier to the poling circuit (b) Optical microscope observation of a periodically poled lithium niobate substrate

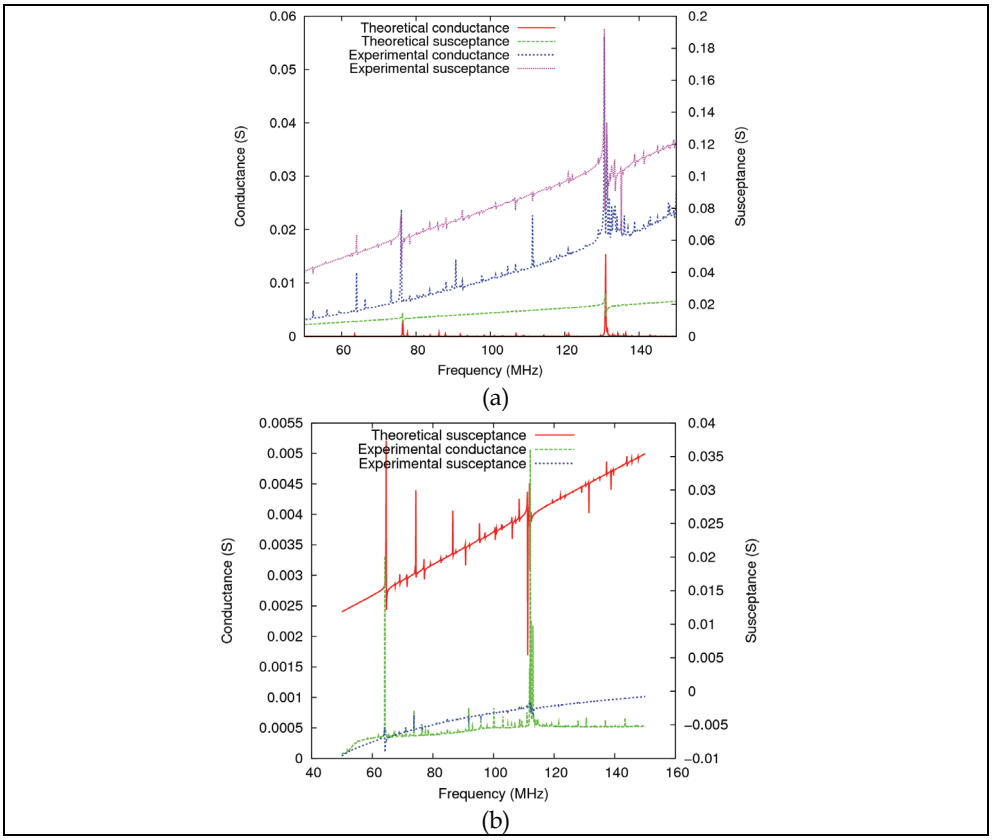


Fig. 5. Theory/experiment assessment for a Lamb wave multi-mode device with 50µm of poling period built on a Z-cut $LiNbO_3$ plate (a) and a Z-cut $LiTaO_3$ plate (b)

3.2 Wafer bonding and lapping/polishing of ferroelectrics upper-layer

The process is based on the bonding of two single-crystal wafers. In this approach, optical quality polished surfaces are mandatory to favor the wafer bonding. A Chromium and Gold thin layer deposition is first achieved by sputtering on both ferroelectrics ($LiNbO_3$ or $LiTaO_3$) and Silicon wafers. Both wafers then are pre-bonded by a mechanical compression of their metalized surfaces into an EVG wafer bonding machine as shown in Fig.6. During this process, we heat the material stack at a temperature of 30°C and we apply a pressure of $65N.cm^{-2}$ to the whole contact surface. The bonding can be particularly controlled by adjusting the process duration and various parameters such as the applied pressure, the process temperature, the quality of the vacuum during the process, etc. We actually restrict the process temperature near a value close to the final thermal conditions seen by the device in operation. Since Silicon and ferroelectrics materials have different thermal expansion coefficients, one must account for differential thermo-elastic stresses when bonding both wafers and minimize them as much as possible. A variant to this process has been tested recently, based on the use of a megasonic cleaning pre-bonder, allowing to significantly reduce the number of bonding defects. Once the pre-bonding achieved, we finish the

bonding process by applying a strong pressure to the stack which eliminates most of the bonding defects not due to dusts and organic impurities (the later being eliminated by the megasonic cleaning), yielding 90% bonded surface and even more.

Fig. 6. Wafer bonding: EVG bonding machine used for wafer pre-bonding (the bonding is finished using a classical press)

Once the bonding achieved, it is necessary to characterize the adhesion quality. Due to the thickness of the wafers and the opacity of the stack (metal layers, Silicon), optical measurements are poorly practicable. As we want to avoid destructive controls of the material stack, ultrasonic techniques have been particularly considered here. The reliability of the bonding then is analyzed by ultrasonic transmission in a liquid environment. The bonded wafers are immersed in a water tank and the whole wafer stack surface is scanned. Fig. 7 presents a photography of the bench. Two focalized transducers are used as acoustic emitter and receiver. They are manufactured by SONAXIS with a central frequency close to 15 MHz, a 19mm active diameter and a 30mm focal length. The beam diameter at focal distance at -6dB is about 200µm. Finally Fig.8 shows an example of bonding characterization. One can see that the bonding is homogeneous and presents few defects. The surface can be considered as bonded (and specially the area of the PPT one can hardly distinguish).

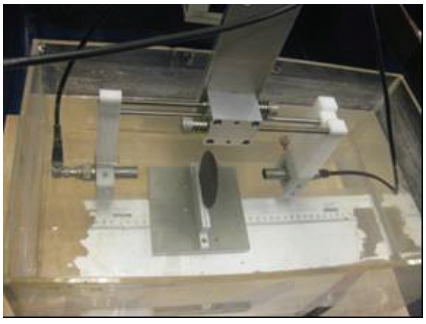


Fig. 7. Ultrasonic tank for bonding characterization based on acoustic transmission (any defect in the path of the ultrasonics beam scatters the pressure wave)

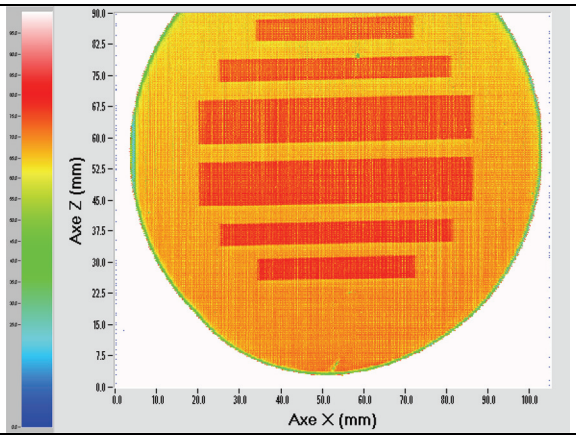
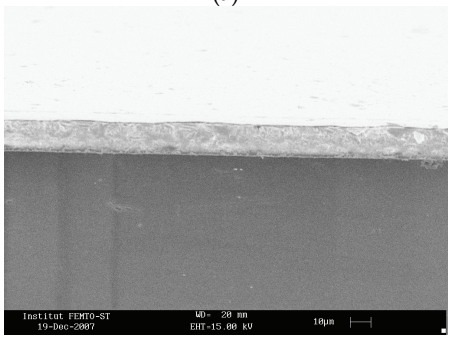


Fig. 8. Example of Si/Lithium niobate bonded surface (4-inch wafers), characterized using ultrasound transmission (Fig. 7)

(a)



(b)

Fig. 9. Photograph of the SOMOS equipment used for lapping/.polishing operations (a) and SEM view of a lithium niobate wafer bonded on a silicon wafer and finally lapped down to about 10µm (b)

The piezoelectric wafer is subsequently thinned by a lapping step to an overall thickness of 100 microns. The lapping machine used in that purpose and shown in fig.9 is a SOMOS double side lapping/polishing machine based on a planetary motion of the wafers (up to 4" diameter) to promote abrasion homogeneity. We use an abrasive solution of silicon carbide. We can control the speed of the lapping by choosing the speed of rotation, the load on the wafer, the rate of flow or the concentration of the abrasive. It is then followed by a micro-polishing step. This step uses similar equipment dedicated to polishing operation and hence using abrasive solution with smaller grain. Fig. 9 shows the equipment used to lap and polish the piezoelectric material and an example of a $LiNbO_3$ layer thinned down to a few tenth of microns, bonded on Silicon.

4. PPT/Si wave-guides

Therefore, waveguides based on a thinned $LiNbO_3$ or $LiTaO_3$ plate bounded on Silicon have been implemented along the flow chart of fig.10, taking advantage of the acoustic velocities in silicon higher than in the above-mentioned materials to meet the guiding conditions. Here again (as shown in fig.11), the accordance between experimental measurements and theoretical predictions confirms the control of the device operation and allows for developing design process.

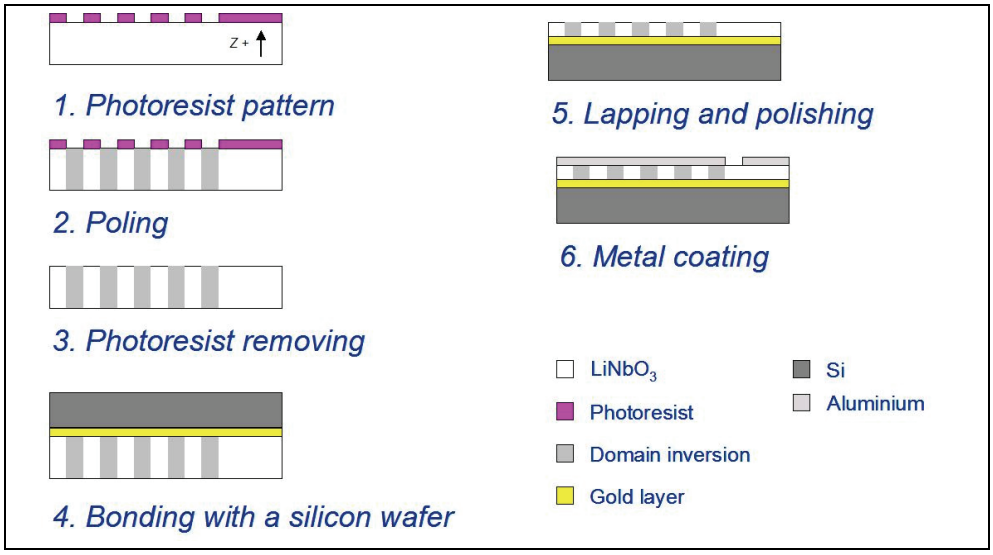


Fig. 10. Flow chart of the fabrication of PPT/Si waveguide

Fig. 12 presents another comparison between measured responses of the implemented devices and the theoretical harmonic admittances obtained with our periodic finite element code. The $LiNbO_3$ layer thickness has been measured for the devices, allowing for accurate computations based on realistic parameters. Here are the results for the 40µm period devices. Since the implemented single-port test devices are quite long and almost behave as single port resonators, the comparison between measurement and harmonic admittance results makes sense.

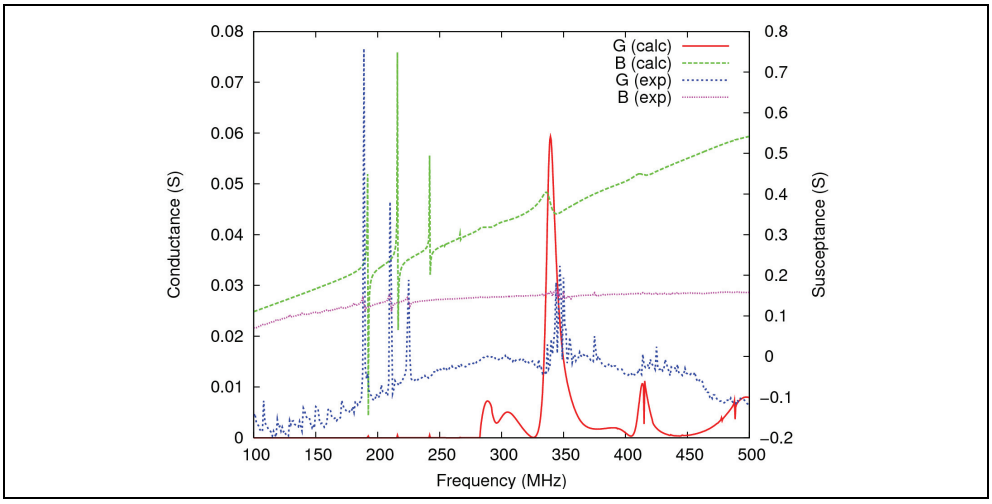


Fig. 11. Theory/experiment comparison for a 20µm period PPT on Silicon ($LiNbO_3$ thickness = 26µm)

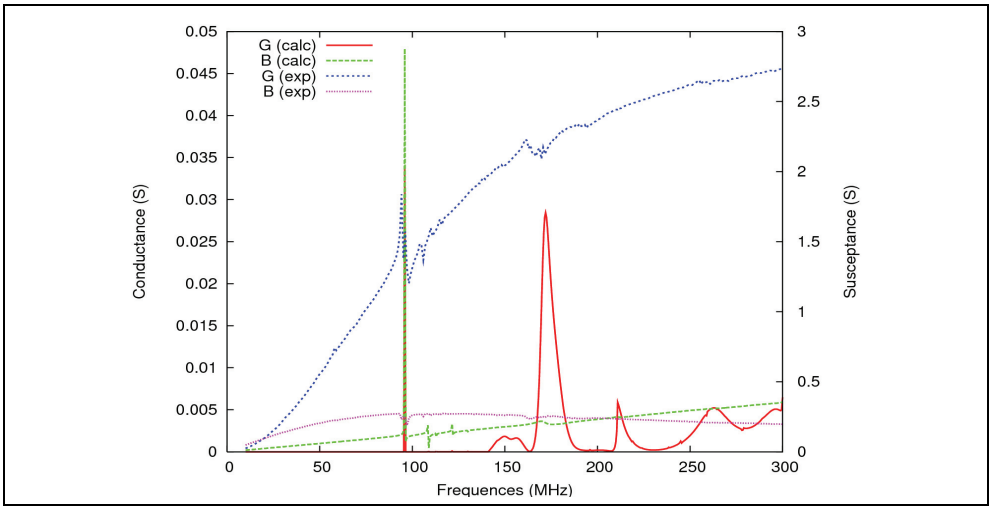


Fig. 12. Theory/experiment assessment for a 40 µm period PPT ($LiNbO_3$ thickness = 50 µm)

5. Si/PPT/SI-based waveguide, resonator and oscillator

Finally, we have developed an isolated wave guide allowing for the propagation of acoustic waves within a PPT plate in between two silicon substrates, yielding advanced packaging opportunities. Fig. 13 illustrates this configuration and Fig.14 shows the kind of theoretical prediction one can obtained using FEM/BEM harmonic computations to demonstrate the targeted guiding effect.

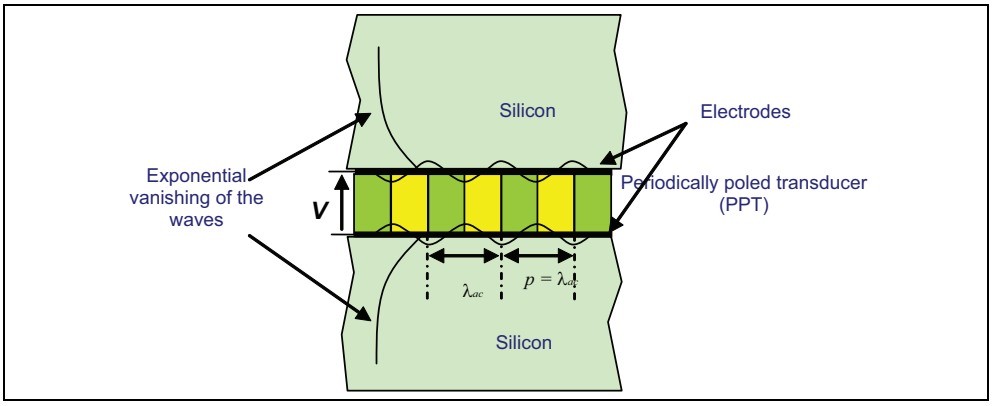


Fig. 13. Principle of the PPT isolated wave transducer

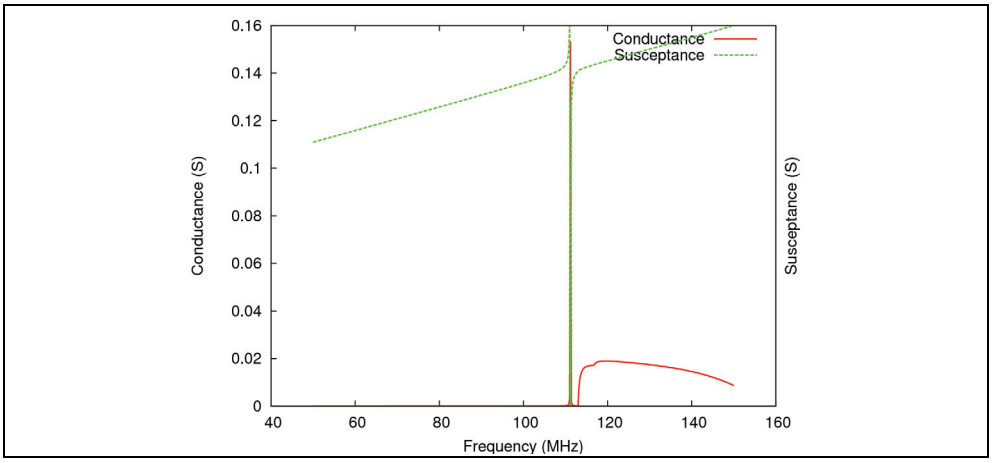


Fig. 14. Example of harmonic admittance computed for a Si/$LiNbO_3$/Si transducer/waveguide, the period of the PPT (wavelength) is 50µm, the niobate layer is 30µm thick (the pole is the signature of a guided mode).

The fabrication of acoustic waveguides based on PPTs consists in bonding a silicon wafer on each side of the periodically poled wafer, as described in fig. 15. In that purpose, the 500 µm thick Z cut lithium niobate wafer is poled and bonded on a (100) 3" doped silicon wafer using a wafer bonding technique developed in our group based on a metal-metal adhesion at room temperature promoted by a high pressure applied to the material stack (Fig.15). The study of the dispersion properties enables to define a specific configuration using a thinned PPT layer of about 30 µm. The $LiNbO_3$ wafer thinning is achieved by home-made lapping and polishing techniques. After this step, the stack of Si(380 µm)/$LiNbO_3$(20 µm) is bonded again on a doped silicon wafer with the same properties that the first one (Fig.16). Several devices have been built along this approach but we mainly have focused our attention on thicker structures (using 500µm thick lithium niobate wafers) for characterization and application purposes.

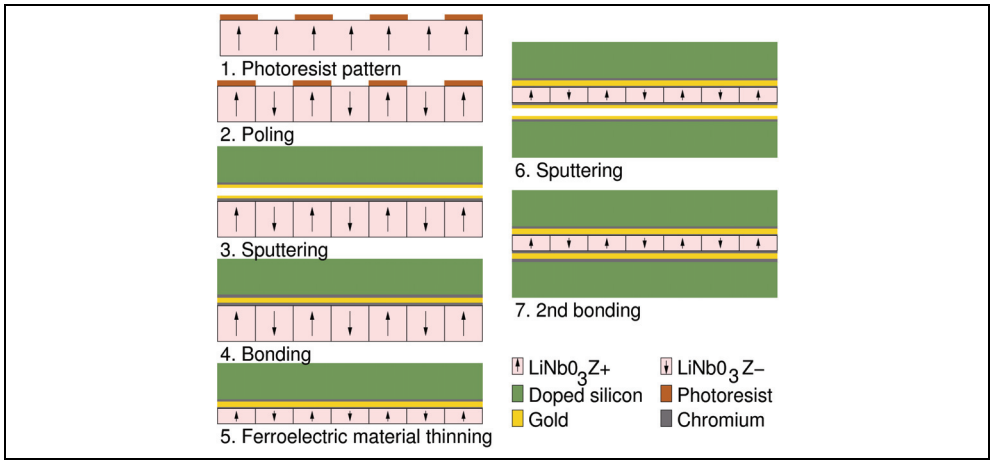


Fig. 15. Flowchart which summarizes the different steps of fabrication

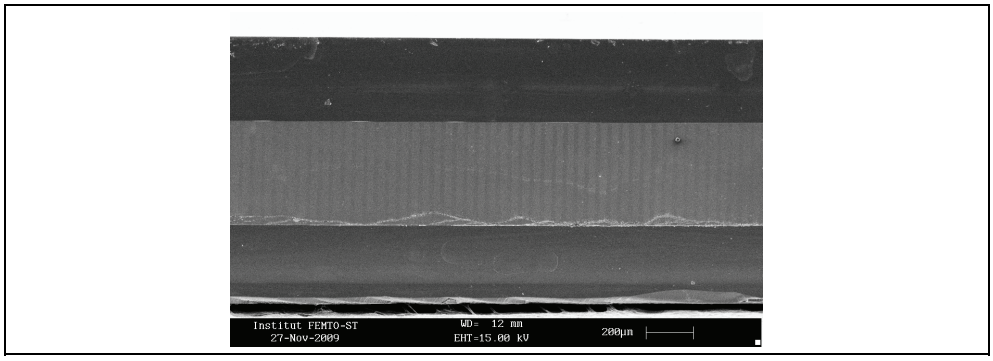


Fig. 16. SEM view of a Si/PPT/SI transducer, clearly showing the periodic poling of the transducer

Operational test vehicles have been achieved using doped silicon wafers to ease the electrical contact. The transducer was built in lithium niobate with a 50 µm period and a thickness equal to 500 µm. Theoretical and measured electrical admittances agree well and allow for identifying a main contribution corresponding to a guided longitudinal mode at 131 MHz (fig. 17). The corresponding phase velocity is very close to the one of the PPT alone (i.e. 6500 $m.s^{-1}$). The elliptically polarized mode excited using the PPT alone and exhibiting a phase velocity of about 3800 $m.s^{-1}$ is not excited nor guided in this configuration. This mode actually needs a free surface to satisfy its boundary conditions (similarly to a Rayleigh wave) and therefore, the existence of rigid boundary conditions on each side of the PPT prevents its excitation and propagation.
This resonator operating near 131 MHz exhibits a quality factor of 13000 and an electromechanical coupling k_s^2 equal to 0.25 % (twice higher than the one of a SAW resonator on Quartz). The corresponding phase rotation (320°) and the dynamic of its electrical reflection coefficient (S_{11}=-8 dB) are suitable for oscillator applications. Such a device therefore has been built using a negative resistance scheme (the so-called Colpitts circuit [Colpitts]).

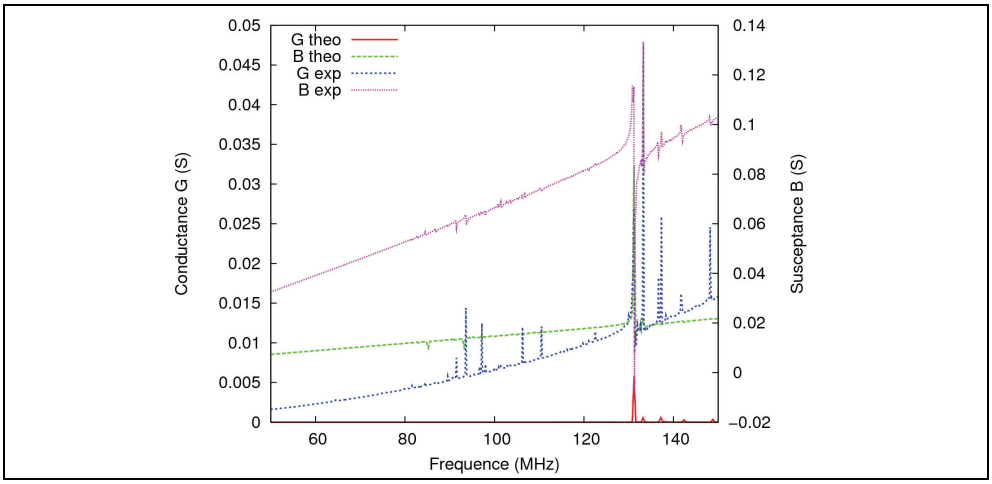


Fig. 17. Theoretical and experimental admittances of a Si(380µm)/$LiNbO_3$(500µm) PPT/Si(380µm) sandwich

A specific printed circuit has been built in that matter (Fig.18). Note that thanks to the isolation of the mode, one could glue the resonator directly on the board allowing for easily grounding the device. A single gold wire then is used to connect the resonator to the oscillator (such a connection yields a notable sensitivity to RF parasites and hence will be improved in the next future). The phase noise of the oscillator at 100 kHz from the carrier shows a value less than -160 dBc/Hz, which can be honestly compared with other acoustic wave oscillators at such frequency, accounting for the fact that the device was excited with a quite low signal level (-6dBm). Therefore, increasing the excitation should allow for a significant reduction of the noise floor and then advantageously compete with standard solutions. Moreover, as the wave guide appears really robust concerning packaging and back end conditioning, it can be integrated more easily than any other acoustic wave based solutions and benefit from a clear applicative potential.

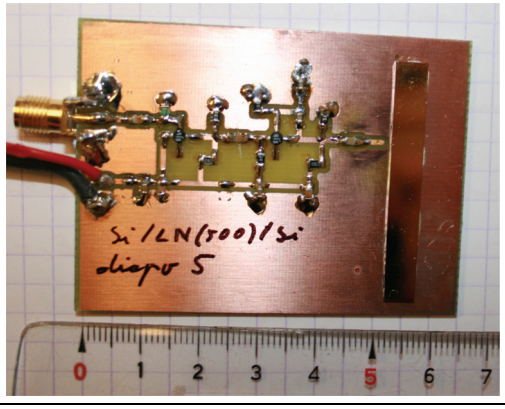


Fig. 18. The oscillator board implemented for phase noise tests

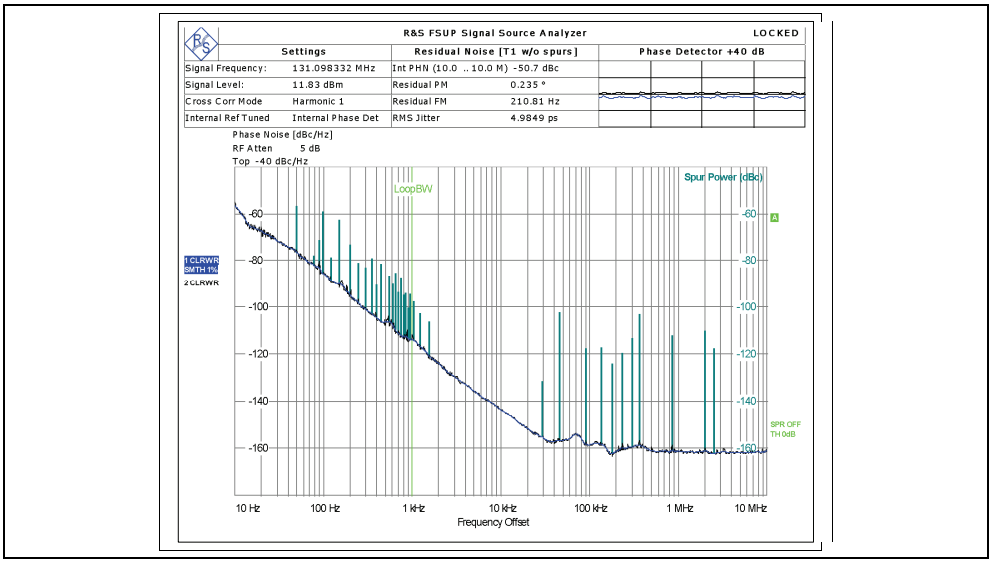


Fig. 19. Phase noise of the 131 MHz oscillator stabilized with a Si/PPt/Si resonator. The noise floor is better than -160 dBc/Hz.

6. Conclusion

In this chapter, we have discussed the standard techniques implemented for optimizing PPTs for fabricating test vehicles and we have proposed a detailed analysis of the experimental tests. We propose some guidelines for future developments and implementation of these new waveguide principles to answer the requirements for the next generation of passive signal processing components, and more particularly resonators and filters. However, because of its very particular configuration, the Si/PPT/Si structure is considered as a potential candidate for sensor applications, particularly when the sensor is expected to be inserted in hosting bodies submitted to parametric perturbations such as stress, vibration or pressure. In that case, the device can be connected directly to the proof body without the need to protect any surface, providing therefore more robustness than SAWs or even bulk-wave-based sensors.

7. Acknowledgment

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8. References

S. Ballandras et al, (2003); A novel surface wave transducer based on periodically poled piezoelectric domain, Frequency Control Symposium and PDA Exhibition Jointly with the 17th European Frequency and Time Forum, 2003. Proceedings of the 2003 IEEE International, vol., no., pp. 893- 896

S. Ballandras et al., (2009) A mixed finite element/boundary element approach to simulate complex guided elastic wave periodic transducers. Journal of Applied Physics 105 1 014911

F. Bassignot et al, (2011) A New Acoustic Resonator Concept Based on Acoustic Waveguides Using Silicon/Periodically Poled Transducer/Silicon Structures for RF Applications, IEEE IFCS, San Francisco

P. Bradley et al, (2000), "Film bulk acoustic resonator (FBAR) duplexer"-- U.S. Patent (USP) #6262637; Agilent inventors Paul Bradley, John Larson, Richard Ruby).

E. Courjon et al, (2007) Lamb wave transducers built on periodically poled Z-cut LiNbO3 wafers, Journal of Applied Physics, 102, 114107

E. Courjon et al, (2008) Characterization of guided modes excited by periodically poled transducers on Si," Frequency Control Symposium, 2008 IEEE International , vol., no., pp.604-608

O. Elmazria et al, (2009), AlN/ZnO/diamond structure combining isolated and surface acoustic waves, Applied Physics Letters, vol.95, no.23, pp.233503-233503-3

D. Gachon et al, (2008) Fabrication of High, Frequency Bulk Acoustic Wave Resonator Using Thinned Single−Crystal Lithium Niobate Layers, Ferroelectrics, Vol.362, n°1, pp. 30−40

D. Gachon et al. (2010) Prediction and Measurement of Boundary Waves at the Interface Between LiNbO3 and Silicon. IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control57 7 1655−1663

J.A. Greer et al, (1990) Metalllisations for Surface Acoustic Wave Resonators: film properties and device characteristics, Proc. of the IEEE Ultrasonics Symposium, Vol.1, pp.483-491

G.F. Iriarte et al, (2003) SAW COM parameter extraction in AlN/diamond layered structures, IEEE Trans. on UFFC, Vol. 50, N°11, pp. 1142–1547

K. Higaki et al, (1997) High power durability of diamond surface acoustic wave filter, Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , vol.44, no.6, pp.1395-1400

M. Kadota et al, (2009) Acoustic Wave Devices using Periodical Poled Z-cut $LiTaO_3$ Plate, Proc. of the joint IEEE IFCS-EFTF, Besançon, pp919-922, 2009

H. Kando et al (2006) 6B-4 RF Filter using Boundary Acoustic Wave, Ultrasonics Symposium, IEEE, vol., no., pp.188-191

R. Lanz, P. Muralt, (2005) Band pass filters for 8 GHz using solidly mounted Bulk Acoustic Wave Resonators, IEEE Trans. on UFFC, Vol. 52, N°6, pp. 946–946

K.M. Lakin, (2003) "Thin film resonator technology", Proc. of the joint IEEE IFCS-EFTF, pp. 1-14

D.P. Morgan, (1985) Surface Wave Devices for Signal processing, Studies in Electrical Eng. 19, Elsevier Ed.

L. E. Myers et al, (1995) Quasi-phase-matched optical parametric oscillator", JOSA B, Vol. 12, Issue 11, pp. 2102-2116

R. Salut & al, (2010) Fabrication of GHz Range Oscillators Stabilized by Nano-Carbon-Diamond-Based Surfcae Acoustic Resonators, Proc of the IEEE International Ultrasonics Symposium, San Diego

A. K. Sarin Kumar et al (2004), High-frequency surface acoustic wave device based on thin-film piezoelectric interdigital transducers, Appl. Phys. Lett. 85, 1757 doi:10.1063/1.1787897 (*3 pages*)

M. Wilm et al, (2002) A full 3D plane-wave-expansion model of 1-3 piezoelectric composite structures, J. Acoust. Soc. Am., vol. 112, n°3, pp. 943-952

4

Ferroelectric Polymer for Bio-Sonar Replica

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1. Introduction

The sensorial knowledge paradigm has captured the interest of many eminent scholars in past centuries (the philosophical trend of "*Sensism*" was developed around the "*Gnoseologic Paradigm*", which has found its highest expression in Étienne Bonnot de Condillac, 1930) as well as in the modern era, particularly in the attempt to interface the external environment to humans through artificial systems. Of the five human senses, which have been investigated by scientists involved in artificial perception studies, vision, touch and hearing have received the most attention, each one for different reasons. When referring to hearing as the sense which perceives sound (the mechanical perturbation induced in a medium by a travelling wave at suitable frequency), a distinction should be made. Indeed, sound between 100 Hz and 18 kHz refers mainly to the range of human perception, while infrasound (up to 20 or 30 Hz) and low frequency ultrasound (from 20 to 120 kHz) refer to animal (mammalian) perception.
Low frequency ultrasounds have been amply investigated in the last century and the resulting applications have been made in both military and civil fields. In any case, it appears relevant and necessary to improve the performance of the ultrasonic system (more properly named sonar) for use in a variety of industrial, robotic, and medical applications where ranging plays a basilar role. Nevertheless, other important information can be extrapolated through proper use of the ultrasonic signal as is evident from the study of the biology and mammalian behaviour (Altringham, 1996). Up to now, attempts have been made to try to emulate animal auditory systems by using both commercial or custom piezoelectric transducers. In this context, the latest investigation in artificial perception was mainly inspired by bat bio-sonar, which has been extensively studied and described by biologists.
As a result of the damping exerted by the propagation medium, which increases as the ultrasound frequency increases, conventional transducers normally function at relatively low frequencies (40 ÷ 50 kHz) in air. Sometimes this restricts choices of piezoelectric materials, besides transducer shape and dimensions. In order to increase the frequency and hence to improve the performances of ultrasonic transducers, flexible plastic materials, such as the ferroelectric polymer polyvinylidene fluoride (PVDF) were investigated and assembled in different geometries. It was discovered that, when properly shaped, PVDF films can resonate at frequencies superior to 100 kHz, covering the full range frequency of the majority of bat bio-sonars (20 ÷ 120 kHz).
The first part of a work aimed at emulating the auditory system of Pteronotus Parnellii, (also known as the *moustached bat*) is described in this chapter. We have simulated some of this

bat's most important strategies, based on the techniques used by its sophisticated echo-location system in gathering ultrasonic information. Specifically, in this phase of the study, the piezoelectric transducer is used to emulate the function of the bat cochlea in a real distance measurement, although bio-sonar capabilities are far superior.
The chapter is organized as follows: first the design and characterization of the ferroelectric polymer ultrasonic transducer is discussed. Based on the piezoelectric equilibrium rules, a suitable transducer geometry has been designed in order to improve the device's performance in air.
Then the transducer impedance has been characterized from 30 to 40 kHz up to 120 kHz, exactly in the same range frequency in which most bat bio-sonars operate. The design of the electronic circuits and the matching of the electric impedance with the ultrasonic transducer received particular attention because of the inherent noise of the PVDF. The sensory unit operates at distances of 10 ÷ 2500 mm with an axial resolution of about 2 mm down to 500 μm. A critical comparison between the custom transducer (based on ferroelectric polymer technology) and similar devices (based on different, but standard, technologies) is also carried out.
These and other problems are considered in this work, including a neural network approach carried out in order to verify the potentiality of the PVDF electronic sonar and the analogism with the bat bio-sonar, in all its complexity, with the aim of exploring how artificial perception in the acoustic field can support human sensorial perception.

Nomenclature

c	Stiffness coefficient	$[N \cdot m^{-2}]$
d	Piezoelectric constant	$[C \cdot N^{-1}]$
C	Capacitance	$[F]$
D	Normal electric displacement	$[C \cdot m^{-2}]$
e	Piezoelectric constant	$[C \cdot m^{-2}]$
E	Electric field	$[V \cdot m^{-1}]$
f	Frequency	$[Hz]$
g	Piezoelectric constant	$[V \cdot m \cdot N^{-1}]$
h	Piezoelectric constant	$[V \cdot m^{-1}]$
I	Electric current	$[A]$
k	Piezoelectric coupling factor	
L	Inductance	$[H]$
M	Figure of merit	
P	Polarization	$[C \cdot m^{-2}]$
Q	Quality factor	
R	Resistance	$[\Omega]$
r	Bending radius	$[m]$
S	Strain	
s	Elastic compliance	$[m^2 \cdot N^{-1}]$
T	Tangential stress	$[N \cdot m^{-2}]$
β	Dielectric impermeabilities	$[m \cdot F^{-1}]$
ε	Permittivity	$[F \cdot m^{-1}]$
ε_r	Relative permittivity	
ε_0	Vacuum permittivity	$[F \cdot m^{-1}]$

φ	Angle	[deg]
SNR	Signal-to-noise ratio	

2. PVDF transducer analogy to bat cochleas

The auditory system of mammals is characterized by a common basic layout in which one can identify three anatomical regions—the external and middle ears (air filled) and the inner ear (filled with biological fluid). The acoustic waves are received, conveyed, and amplified by the external and middle ears, while the vibrational energy related to sound pressure is converted into bio-electric energy by the inner ear. Sound amplification is carried out mechanically by a system which includes the ossicles: the malleus, the incus, and the stapes; and the eardrum.

In the system we propose for bio-sonar replication, the amplification of the signal and all other steps included in acoustical signal conditioning are carried out electronically, while the piezoelectric transducer is concerned with the conversion of mechanical energy. Our attention was focalized on the third anatomic region, particularly the cochlea, which transduces mechanical energy into bio-electrical energy, and the acoustic nerve, which carries the bio-electrical signal to the cerebral cortex.

In this section the anatomic structure of the cochlea and its working is reviewed in order to clarify and justify the choice concerning materials, particularly the ferroelectric polymer, and methods used to emulate the bio-sonar of bats.

The cochlea of a bat, similar to that of other mammals, boasts a hollow spiral geometry divided into three channels; the vestibular and tympanic channels are filled with endolymph, which is very similar to intracellular liquid, and the middle channel is filled with perilymph, similar to extracellular liquid, each one separated by an endothelial membrane (see Figure 1). As far as the electronic system is concerned, the most important component is the basilar membrane which, through vibration, activates the receptors of the organ of Corti, that lie over it (the organ of Corti includes the tectorial membrane, two different systems of hair cells, and nervous fibres; these generate bio-pulses as a consequence of the vibration).

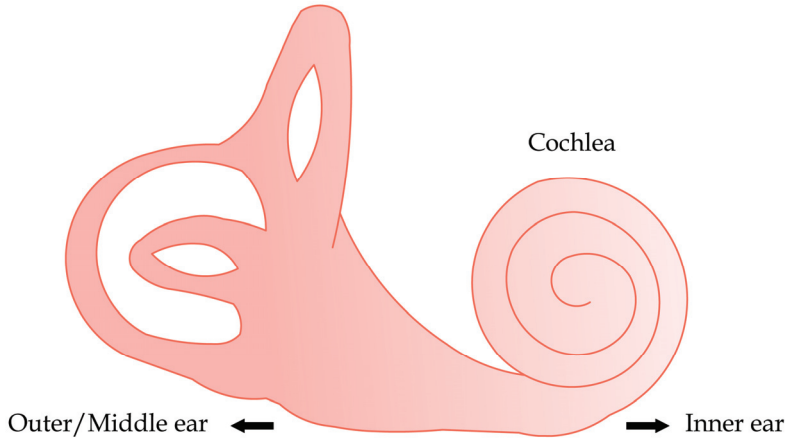


Fig. 1. Main part of the inner ear and arrangement of cochlear component.

When the acoustic wave reaches the eardrum after passing through the outer ear canal, it has already been primarily amplified in this resonant cavity of the external ear. Successively it is mechanically amplified in the middle ear by the chain of ossicles acting as levers on the oval window, located in the inner ear. The travelling wave, once in the cochlea, propagates along the basilar membrane (see Figure 2), which acts as a mechanical filter with respect to the frequency spectrum. Different frequency components of the signal cause the motion of different parts of the membrane in a tonotopic organization. The behaviour of the basilar membrane is related to its geometry, because moving from the base toward the apex the membrane increases its width and thickness, while the resonance frequency decreases.

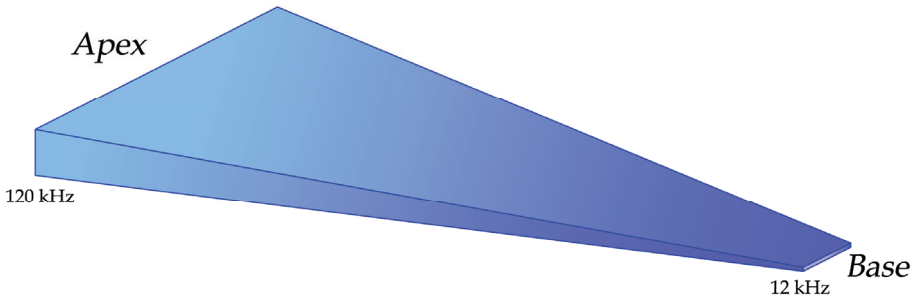


Fig. 2. Basilar membrane winding inside the cochlea

The receptors located in the organ of Corti are divided into outer and inner hair cells, and perform two different functions. The motion of the basilar membrane intimately connected to the organ of Corti is first amplified by the outer hair cells and then transmitted through the liquid to the tectorial membrane that induces the deflection of the hair in the inner cells. The inner hair cells transduce the mechanical signal, after amplification, into an electrochemical signal through the activation of ionic channels and the release of a neurotransmitter (glutamate) to the acoustic nerve, as a consequence of the polarization level of the cells itself. The neurotransmitter reaches the central nervous system through the *afferent fibres*, which account for 90 ÷ 95 % of the total connections, while the rest are connected to the inner hair cells. From the bio-electrical point of view, this process is concerned with the generation of an action potential which drives ionic currents along the axons of the *afferent fibres* (see Figure 3); conversely, the majority of the *efferent fibres* connect the central nervous system to the outer hair cells.
Referring to the analogism with the artificial system, the PVDF ultrasonic transducer acts in a way similar to the basilar membrane, except for the absence of the outer hair cells. In effect though, the acoustic pressure is not mechanically amplified, but merely converted, by the direct piezoelectric effect , into an electrical signal and, hence, only *afferent electronic pathways* are considered. PVDF is a light and flexible plastic material, of several tens of μm in thickness, which can be shaped into hemicylindrical geometries in order to fabricate the ultrasonic transducer which resonates in the frequency range of bat biosonar. The resonance frequency is inversely proportional to the bending radius and can be easily tuned to the suitable values necessary for the specific tasks accomplished by the bat. In fact the curved PVDF ultrasonic transducer works in a way similar to the basilar membrane.

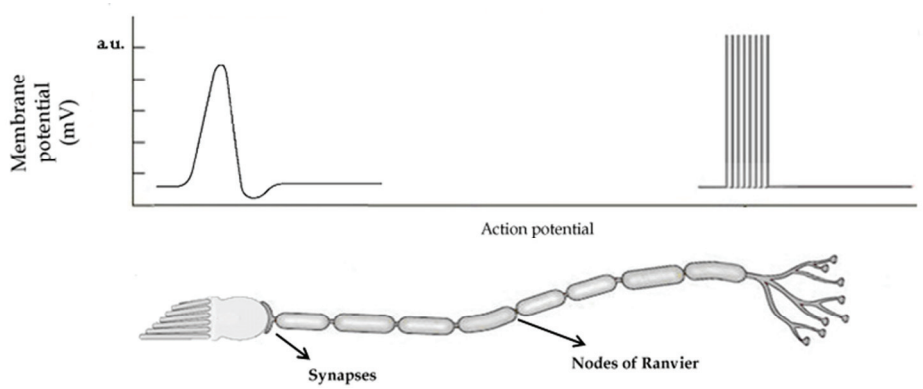


Fig. 3. Structure of hair cell and axon with generated potential along it. The synapses carries the neurotransmitter molecules through the axon. The nodes of Ranvier refresh action potential through the pathway.

The electric dipoles in piezo-polymer, upon the application of an external pressure, generate a net electric charge (which is conveyed through the *afferent electronic pathways* to the central processing system); the inner hair cells also generate a bio-electrical stimulus upon deflection of the basilar membrane. In the next section of this chapter we briefly introduce the ferroelectric phenomenon in PVDF with emphasis on the piezoelectric effect and we describe the design and characterization of the ultrasonic transducer.

3. Polyvinylidene fluoride (PVDF) polymer

To understand the behaviour of ferroelectric materials and their field of application as sensors, we look at both the piezoelectric and pyroelectric effects. Crystals without centers of symmetry may have one or more polar axes and show both vectorial and tensorial properties. Since they exhibit spontaneous polarization, they are defined polar crystals, which display a pyroelectric effect, that is, a change in polarization under a gradient of temperature (Jona & Shirane, 1962; Berlincourt, 1981). In addition, polar crystals exhibit both a direct piezoelectric effect (a state of electrification caused by a mechanical deformation) and a converse piezoelectric effect (a mechanical deformation caused by the exertion of an external electric field) (Curie, 1880). At the end of the 60's, the discovery of strong piezoelectric (Kawai, 1969) and pyroelectric activity (Bergman et al., 1971) in PVDF ascribed the polymer to the family of synthetic ferroelectric polycrystals.

3.1 Atomic structure and morphology

Polyvinylidene fluoride is a semicrystalline linear polymer, with long molecular chains in which each monomer $\left[-CH_2-CF_2-\right]$ has a dipole moment. It is synthesized in poly-crystalline forms, the most important of which are the α and β forms shown in Figure 4. In the α form (or form II), obtained by fusion, the lattice has a monoclinic unit cell with 2/m symmetry and contains trans-gauche/trans-gauche molecular conformation (TGTG'). The β form (or form I) is obtained from the α form by low temperature stretching. In this case, the lattice unit cell is orthorhombic with mm2 symmetry and all-trans zigzag molecular

conformation (TTTT). Unlike the α antipolar crystal form, the β form is piezoelectric and exhibits spontaneous polarization. Although there are two other crystalline structures α_p and γ, for technological purposes the β form is the most interesting due to its stronger piezoelectric and pyroelectric properties (Davis, 1988).

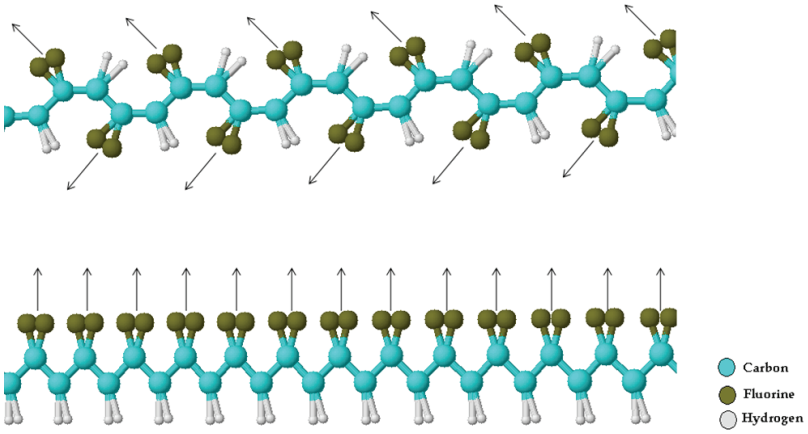


Fig. 4. Representation of crystalline α (upper) and β (lower) forms. Arrows indicate the orientation of the dipole moment.

3.2 Poling methods

Because of its molecular conformation, unoriented PVDF in the α form does not exhibit large piezoelectric and pyroelectric coefficients. In order to induce reproducible ferroelectric characteristics, the polymer must be oriented and poled (a higher degree of orientation results in increased piezoelectric activity). There are several techniques for poling PVDF including: corona poling, thermal poling, plasma and higher electric field poling, and simultaneous poling/stretching techniques. Starting with a non-polar α form, the polymer film is heated to 50 ÷ 60 °C and then uniaxially stretched along direction 1 called the "Machine Direction" or alternatively stretched biaxially along direction 2, called the "Transverse Direction", as shown in Figure 5. Stretching recrystallizes the PVDF in the β form, which renders it suitable to be poled using some of the previously mentioned techniques.

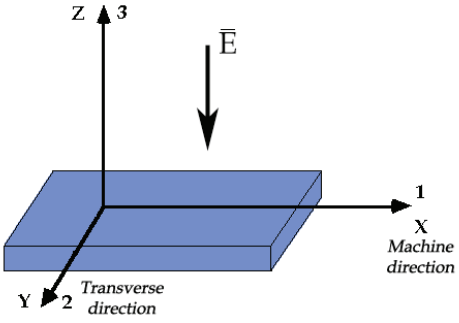


Fig. 5. Fundamental directions of PVDF film

The corona discharge is a room-temperature poling technique accomplished by applying high voltage to the PVDF film, placed between a flat electrode and an array of conductive tips placed at a distance of a few millimeters with an interposed control grid. The poling process is completed within several seconds and a high temperature was found to yield greater and more stable piezoelectric and pyroelectric effects (Bloomfield et al., 1987). Poling can also be carried out by applying electric fields, between 500 kV/cm and 800 kV/cm at high temperatures (90 ÷ 110 °C) for about one hour; the electric fields must be applied directly to both the metalized faces of the film. High temperatures create thermal agitation, allowing a partial alignment of the dipoles due to the electric field. Successively, the temperature is decreased and then the electric field switched off, resulting in a permanently polarized state of the polymer (Hasegawa et al., 1972). One of the most utilized methods (Bauer, 1989) is that of applying an alternating electric field through the polymer at a frequency ranging from 0.001 Hz to 1 Hz, while gradually increasing the amplitude of the electric field, which results an hysteresis loop of polarization. This technique allows the achievement of a very stable, reproducible and durable polarization.
Polarization can easily be controlled by monitoring the actual current passing through the polymer which is given by:

$$i = \varepsilon\left(\frac{dE}{dt}\right) + \left(\frac{dP}{dt}\right) + \left(\frac{E}{R}\right) \tag{1}$$

3.3 Piezoelectric equations

A necessary condition to induce piezoelectricity in a medium is the absence of a center of symmetry in its atomic structure. Starting from thermodynamic potential, in adiabatic and isothermal conditions, general piezoelectric equations can be derived. Neglecting the effects of the magnetic field, the most useful simplified equations are given as follows:

$$\begin{cases} S = s^E T + d_t E \\ D = dT + \varepsilon^T E \end{cases}$$
$$\begin{cases} S = s^D T + g_t D \\ E = -gT + \beta^T D \end{cases}$$
$$\begin{cases} T = c^D S - h_t D \\ E = -hS + \beta^S D \end{cases} \tag{2}$$
$$\begin{cases} T = c^E S - \mathrm{e}_t E \\ D = eS + \varepsilon^S E \end{cases}$$

The first pair of equations is the most used, where electric field and stress are taken as independent variables. The second pair of equations can be used for general purposes except for triclinic and monoclinic crystal systems. The last two pairs are used when the strain is prevalent in only one dimension. The four piezoelectric constants are related as follows:

$$d = \left.\frac{\partial S}{\partial E}\right|_T = \left.\frac{\partial D}{\partial T}\right|_E \qquad g = -\left.\frac{\partial E}{\partial T}\right|_D = \left.\frac{\partial S}{\partial D}\right|_T \tag{3}$$

$$e = -\left.\frac{\partial T}{\partial E}\right|_S = \left.\frac{\partial D}{\partial S}\right|_E \qquad h = -\left.\frac{\partial T}{\partial D}\right|_S = \left.\frac{\partial E}{\partial S}\right|_D$$

Below a brief notation in matrix form of the tensor theory for PVDF is reported (Mason, 1964, 1981):

$$\begin{vmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \\ \hline D_1 \\ D_2 \\ D_3 \end{vmatrix} = \left|\begin{array}{cccccc|ccc} s_{11}^E & s_{12}^E & s_{13}^E & 0 & 0 & 0 & 0 & 0 & d_{31} \\ s_{12}^E & s_{11}^E & s_{13}^E & 0 & 0 & 0 & 0 & 0 & d_{31} \\ s_{13}^E & s_{13}^E & s_{44}^E & 0 & 0 & 0 & 0 & 0 & d_{44} \\ 0 & 0 & 0 & s_{44}^E & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & 0 & s_{44}^E & 0 & d_{15} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66}^E & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & d_{15} & 0 & \varepsilon_{11}^T & 0 & 0 \\ 0 & 0 & 0 & d_{15} & 0 & 0 & 0 & \varepsilon_{11}^T & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 & 0 & 0 & \varepsilon_{33}^T \end{array}\right| \cdot \begin{vmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \\ E_1 \\ E_2 \\ E_3 \end{vmatrix} \tag{4}$$

One of the most important properties of piezoelectric materials is their ability to convert energy, expressed by the piezoelectric coupling factor k which is related to the mutual, elastic, and dielectric energy density. It is a useful parameter for the evaluation of power transduction, and is better than the sets of elastic, dielectric and piezoelectric constants.

4. PVDF applications

4.1 Acoustical and optical devices

The most common applications of PVDF are in the fields of electro-acoustic, electro-mechanic (Sessler, 1981; Lovinger, 1982, 1983; Hunt et al., 1983), and pyroelectric transducers (a "vidicon" imaging system was proposed by Yamaka, 1977). In the field of electroacoustic transducers, the ferroelectric polymer was largely used as an ultrasonic transducer in the MHz frequency range for application in the medical field, and in the audio frequency range. In the first case, its functioning principle is based on the thickness mode of vibration along the z direction (see Figure 5), in which one or both of the wide faces are clamped to a rigid bulk, while in the second case, at much lower frequencies, the transverse piezoelectric effect along the x direction is predominant.

Thanks to its piezoelectric characteristics (compared in Table 1 with other piezoelectric materials such as low Q - quality factor - together with low acoustic impedance, lightness, conformability, and very low cost), it is also a competitive material in the fabrication of ultrasonic transducers. It resonates in the thickness mode at very high frequencies, for use in non-destructive testing in clinical medicine (Ohigashi et al., 1984).

Property	Unit	PZT4	PZT5A	PZT5H	$PbNb_2O_6$	PVDF	P(VDF-TrFE)
Sound velocity	m/s	4600	4350	4560	3200	2260	2400
Density	10^3kg/m^3	7.5	7.75	7.5	6.2	1.78	1.88
Acoustic impedance	10^6Rayl	34.5	33.7	34.2	20	4.2	4.51
Elastic constant	10^9N/m	159	159	147	-	9.1	11.3
Electromechanical Coupling Factor k_{31}		0.51	0.49	0.50	0.32	0.2	0.3
Piezoelectric constant							
e_{33}	C/m^2	15.1	15.8	23.8	-	-0.16	-0.23
h_{33}	10^9V/m	2.68	2.15	1.84	-	-2.9	-4.3
d_{33}	pC/N	289	375	593	85	17.5	18
d_{31}	pC/N	-123	-	-	-	25	12.5
g_{33}	V·m/N	0.0251	0.0249	0.0197	0.032	-0.32	-0.38
$\varepsilon_r=\varepsilon_{33}/\varepsilon_0$		635	830	1470	300	6.2	6

Table 1. Comparison of main piezomaterial properties

Another high frequency application is in combination with integrated electronic circuits in the fabrication of a 32-element array configuration for ultrasonic imaging (Swartz and Plummer, 1979).
The performance of transducers realized on silicon was improved by spinning a 15 μm-thin layer of a solution of P(VDF-TrFe) (a copolymer of the polyvinylidene fluoride) in MEK (Methyl Ethyl Ketone), onto a processed silicon wafer in which a low noise NMOS transistor with an extended gate was integrated (Fiorillo et al., 1987).

4.2 Low frequency ultrasound devices

At much lower frequencies, an electric potential applied to both of the wide faces of a free PVDF sheet, generates length-extensional vibrations along x that can be converted into a radial vibration by curvature. This second principle of functioning was exploited in two different ways; the PVDF film is stretched out on a polyurethane support with a small curvature, or alternatively a hemicylindrical shape is imposed to the free sheet by clamping the narrowest sides along direction y at a distance of πr.
The piezoelectric equilibrium of a thin sheet of PVDF, polarized along the z or 3 direction and stretched along the x or 1 direction, is governed by the following equations:

$$\begin{aligned} S_1 &= s_{11}^E T_1 + d_{31} E_3 \\ D_3 &= d_{31} T_1 + \varepsilon_{33}^T E_3 \end{aligned} \tag{5}$$

By applying an alternating voltage between the two electrodes, the hemicylindrical geometry and its lateral constraint allows the conversion of longitudinal motion into radial vibration (see Figure 6). Ultrasonic waves are generated in forward and backward directions. The resonance frequency is inversely proportional to the bending radius and can

be easily controlled by varying it. Neglecting the clamping effects, the resonance frequency is given by:

$$f = \frac{1}{2\pi r}\sqrt{\frac{1}{\rho s_{11}^{E}}} \tag{6}$$

where r is the radius of the curvature and $1/s_{11}^{E}$ and ρ are Young's modulus and mass density of curved PVDF film material, respectively (Fiorillo, 1992). Similar results were verified by finite element analysis (Toda, 2000). However in the curved geometry proposed by Toda and adopted by Hazas & Hopper (2006), clamping generates secondary acoustic fields which result in energy loss and directivity reduction.

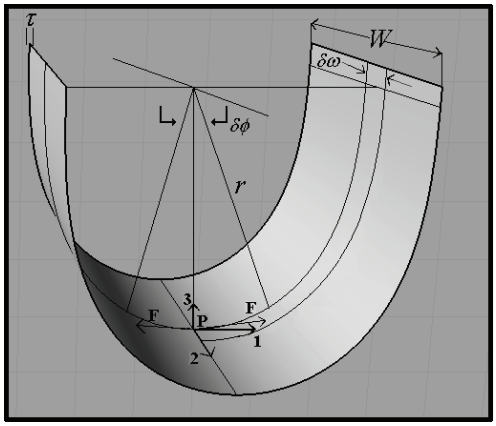


Fig. 6. A piezo-polymer film transducer obtained by curving a PVDF resonator in the length extensional mode along the 1 or stretching direction.

4.3 PVDF transducer modeling

Because of the ferroelectric polymer's inherent noise, a correct modeling of the transducer's electric impedance plays an important role in designing the electronic circuits. In order to design a specific electronic circuit capable of driving the PVDF transducer with high voltage over a wide band centered around the resonance, and of amplifying the echo with a high SNR (signal-to-noise-ratio), a Butterworth- VanDyke modified model has been implemented in the receiver. Both the modulus and the phase of the electric admittance of the transducer have been measured by using an impedance gain-phase analyzer.

Although the piezopolymer transducer suffers from high dielectric losses, the resonance frequency can be determined with good approximation from the phase diagram of the electric admittance. On the other hand, the almost flat diagram of the modulus around the resonance leads to more coarse results that, especially at low US frequency, need further manipulation in order to give reliable information. For instance, at the resonance frequency $f_r = 42.7kHz$, the Butterworth-Van Dike modified model of the electric impedance of the transducer can be characterized by the following parameters: $R_s = 330k\Omega$, $L_s = 10H$, $C_s = 1.4pF$, $R_0 = 210k\Omega$, $C_0 = 248.5pF$, where , R_0 has been introduced in the static branch to take into account dielectric losses as shown in Figure 7.

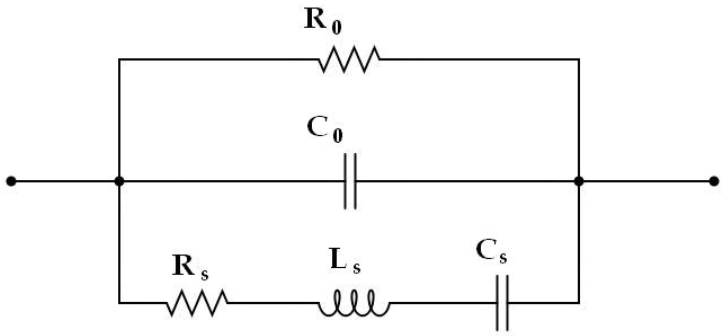


Fig. 7. Impedance equivalent model of the piezo-polymer transducer which also takes into account dielectric losses in which $R_0(\omega)$ and $C_0(\omega)$ are frequency-dependent parameters.

Piezoelectric devices are characterized by the figure of merit $M = k^2 Q$, where k is the electromechanical coupling and Q is the quality factor. In order to radiate or receive acoustical waves, piezoelectric transducers are required to have smaller M characterized by high k but low Q. Because of their inherent properties, piezo-ceramic and standard piezo-crystal sound transducers normally have high electromechanical couplings and high quality factors. We have modified the structure in order to increase the bandwidth and to further reduce the quality factor Q, while the resonance frequency can be continuously changed by modifying the film bending radius. As a result we obtained a controlled resonance transducer with a very low synthetic quality factor for choosing the right axial resolution and improving the pulse echo mode functioning over the full range frequency of bat biosonar (Fiorillo, 1996).

4.4 PVDF transducer with controlled resonance

In this second assembly, the transducer is realized by curving the sheet, according to parabolic shape, where the two extremities A and B, are tangentially blocked along two lines, t and t', that originate in point O (see Figure 8). The bending of the film is mechanically controlled by changing the opening arc angle ϕ between t and t'. The equation of the parabolic transverse section, $y = -ax^2 + c$, can be rewritten by considering two new parameters: the slope of t(t'), $m = \tan\left[(\pi - \varphi)/2\right]$ (m'=-m) , and d(d'), the fixed distance from the origin O to A (and B, respectively). Then, the arc length l has been evaluated as a function of d(d') and m(m'). Finally the ratio l/d (l/d') at various m(m') values, has been considered. Because of the imposed geometry and in order to assume a parabolic transverse section at any angular position ϕ, the ratio l/d (l/d') must be a constant quantity. Hence the film motion, converted from extensional to radial by geometry, can be studied by considering a parabolic shape in the range $27° < \phi < 40°$ with an error less than 5%. When ϕ=50° the error increases up to 10%. By increasing the length l of the film in comparison with d(d'), it is possible to further increase the opening arc angle and, consequently, to reduce the resonance frequency. The transducer shape is now quite different from the parabolic one. However the maximum angle ϕ cannot exceed 70°, without the transducer being damaged.

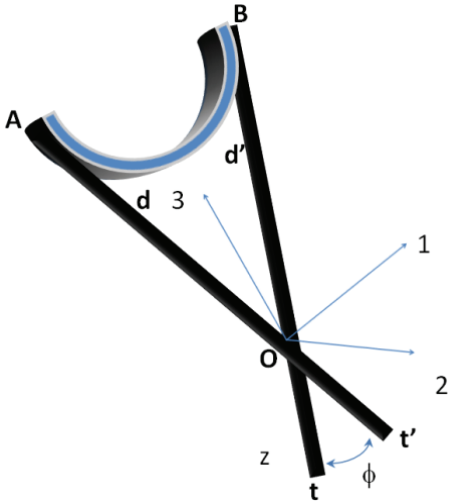
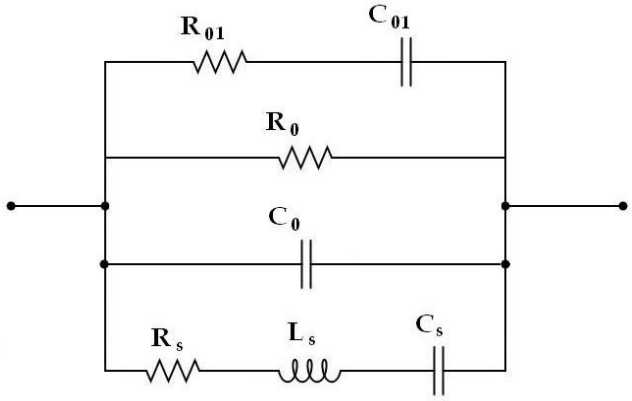


Fig. 8. Three dimensional view of transducer assembling in variable resonance frequency configurations clamped along A and B

ϕ [deg]	27	30	35	40	45	50	55	60	65	67
f_r [kHz]	65.1	61.3	54.6	50.5	47.3	42.7	38.0	35.8	34.3	30.0

Table 2. Resonance frequency vs opening arc angle

Experimental results show that the resonance frequency is inversely proportional to the opening arc angle ϕ between t and t'. It decreases from 65 kHz, when ϕ=27°, to 45 kHz when ϕ=50°. For ϕ>50° the film shape is quite different from a parabolic cylinder, however the resonance frequency decreases to 30 kHz by increasing the opening arc angle to ϕ=67°. These results are in good agreement with previous results obtained using hemicylindrical transducers with circular transverse sections, different bending radii and different lengths.
By considering the upper -3dB frequency f_H≈71.4 kHz and the lower -3dB frequency f_H≈27 kHz (for each angular position it is Q≈5), when ϕ ranges, respectively, from 27° to 67° (see Table 2), a broad-band transducer B=f_H-f_L=44.5 kHz with central frequency of 49.25 kHz and very low synthetic quality factor Q≈1 is obtained.
The immediate advantage of this kind of transducer is the possibility of changing the axial resolution, which can be increased up to λ/50 (c/f, c=344 ms^{-1}, T=24 °C, relative humidity =77%) with digital phase measurement techniques of the transit time of the echo signal, and ranges between 250 μm, at f_L≈27 kHz , and 96 μm, at f_H≈71.5 kHz, for an accurate profile reconstruction up to a distance of 0.5 m. A closer dependence of the resonance frequency from both the bending radius and the opening arc angle, at different arc lengths, as well as a complete electromechanical model of the transducer, has been studied. This model takes into account the high dielectric losses of the piezo-polymer foil, even far from resonance.
Because the polymer's inherent noise also is related to its high dielectric losses, which are frequency dependent, as well as $C_0(\omega)$ and $R_0(\omega)$ (see Figure 7), we modified the parallel connection between C_0 and R_0 to have constant lumped parameters in the static branch over a broad frequency range.



f_r	60.9 kHz
R_{01}	19.0 $k\Omega$
C_{01}	72 pF
R_0	31 $M\Omega$
C_0	217 pF
R_s	290 $k\Omega$
C_s	1.37 pF
L_s	4.6 H
Q	6.1

Fig. 9. RLC equivalent electric circuit of the transducer in which the R C series branch makes the parameters independent of frequency variation in the range 1 kHz-150 kHz.

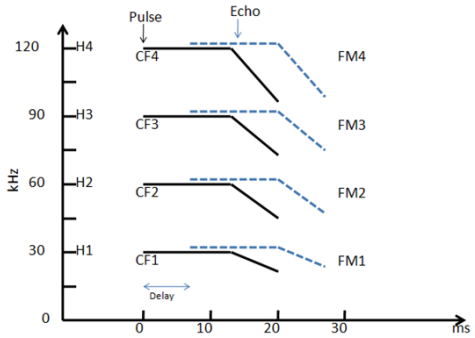
The static side of the equivalent electric circuit was modified by inserting a second branch that includes a resistor (R_{01}) connected in series to a capacitor (C_{01}) as shown in Figure 9. The values of C_0, R_0, C_{01}, R_{01} are approximately constant between 1÷150 kHz. The electric behavior of the two static networks was equivalent in the frequency range of interest. In addition the modified equivalent admittance better approximates the measured values (Fiorillo, 2000). Once we determined the equivalent electrical circuit with constant electric parameters, of the lossy transducer in a relatively broad frequency range, we investigated the pre-amplifier noise sources and the noise generated in the receiver, Rx, to optimize SNR. For this reason we took into account the transducer equivalent electric network with related Johnson noise sources. We did not consider noise sources in the transmitter, Tx, because the driving voltage can be arbitrarily increased within the limits of dielectric breakdown.

5. Echo-location techniques of bat

There are 966 species of bats that use different ultrasonic waveforms to move between obstacles and to locate the target. The most simple bio-pulses are very simple clicks of around 40 kHz. Some species emit constant frequency signals, CF, a sinusoidal burst of many cycles, or frequency modulated signals, FM. Another more sophisticated form of the US signal is a combination of a CF pulse immediately followed by a downward chirp, an FM pulse. This kind of CF-FM, can be a pure tone or a multi-harmonic signal. Its energy may be selectively controlled depending on the distance and the size of the target.

5.1 Echo-location of Pteronotus Parnellii

The most complex CF-FM pulse is that emitted by the Pteronotus Parnellii, or moustached bat, which is composed of four harmonics: the fundamental CF_1-FM_1, at 30.5 kHz, followed by the downward chirp in which the frequency is reduced to 20 kHz, and three higher harmonics, followed by relative chirps, CF_2-FM_2 at 61 kHz, CF_3-FM_3, at 92 kHz, and CF_4-FM_4 at 123 kHz respectively down to about 50, 80, and 110 kHz (see Figure 10a). The mustached bat is able to extract plenty of information from the echo signal as shown in Figure 10b.



a)

Echo	Target
Doppler shift	Velocity
DC component	Relative velocity
AC component	Flutter
Amplitude	Subtended angle
Delay	Range
Amplitude+delay	Size
Amplitude spectrum	Fine characteristic
Binaural cues	Azimuth
Pinna cues	Elevation

b)

Fig. 10. The four pulse components of the bio-signal generated by the mustached bat. In diagram a) the solid line represents the superimposed CF-FM component, while the dashed line depicts the received echo . Table b) shows information received by the bat related to the characteristics of the echo signal analysis.

Distance is evaluated using the echo delay, throughout the time-of-flight (TOF) as related to the frequency modulated components FM_2, FM_3, FM_4. The FM signals are used to cover the whole range of the bio-sonar. In particular the components FM_2, FM_3, FM_4 operate at the maximum, medium and minimum distance, while the first component, FM_1, is used to start the TOF measurement and is sent to the auditory system, internally, through the larynx. A neural network model based on FM-FM neurons and proposed by Suga (1990) is shown in Figure 11. The neural network is mainly divided into two parts:

- An afferent pathway appointed to the transmission of the PFM_1 pulse
- An afferent pathway appointed to the reception of EFM_n (n=2, 3 or 4) echoes

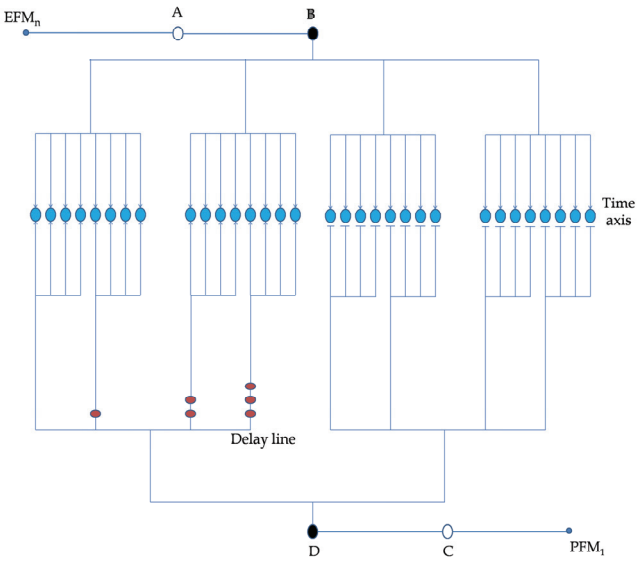


Fig. 11. Scheme of a portion of the neural network for ranging analysis

The neural network compares the first component PFM_1 with each one of the other three EFM_2, EFM_3 and EFM_4, in three different neural structures: one for PFM_1-EFM_2, one for PFM_1-EFM_3 and one for the PFM_1-EFM_4 components. The FM_n (n=2,3 or 4) components of the echo are elaborated by the neural network in order to obtain a sequence of bio-pulses, each one related to a particular delay time. The neurons are located over the delay time axis and are tuned to a particular delay time from 0.4 ms to 18 ms. They receive the echo naturally delayed by the target from the upper network (neurons EFM_n, A, B). This echo reaches all the neurons of the time axis. Similarly the start pulse (PFM_1) reaches each neuron of the time axis from the lower network (neuron PFM_1, C, D) with increasing delay accomplished either with variation in length and axon diameter or by different time inhibition values. In this neural structure only one neuron is excited, by both EFM_n and PFM_1, when the echo and the pulse are combined with a particular delay, and generates an action potential at the time-of-flight as related to target distance.

5.2 The PVDF sonar system and the afferent electronic pathway

The PVDF transducer can be used as a transmitter (converse piezoelectric effect) or a receiver (direct piezoelectric effect) of ultrasonic signals. The circuit for driving the transmitter with CF – FM signals, is realized using a power operational amplifier, followed by a step-up transformer, that generates a wide range of signals from a few volts up to a few hundred volts in both CF and FM mode. The receiver converts ultrasonic energy into electric energy and the signal is firstly pre-amplified with a very low-noise, low-distortion operational amplifier, designed for low frequency ultrasound applications (Fiorillo et al., 2010). It is then filtered and conditioned to be suitable for neural network processing as shown in Figure 12.

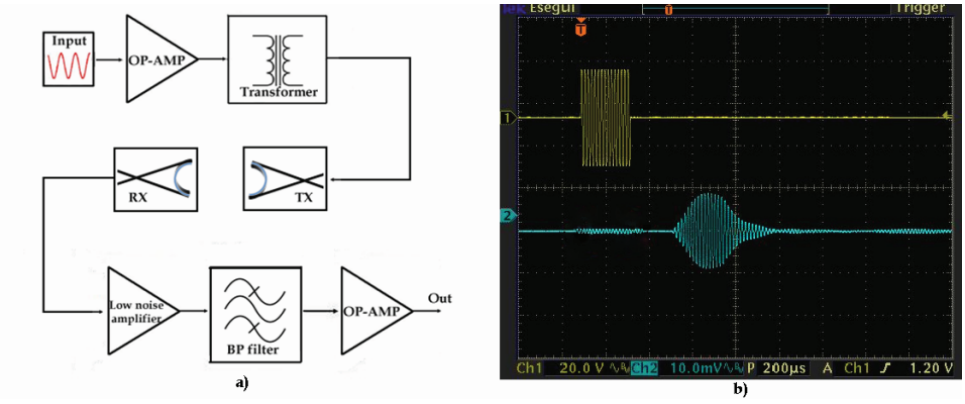


Fig. 12. Block diagram of the transmitter and receiver circuit a). 65 kHz burst signal (upper) reflected by a plane (lower) located at 150 mm from the sonar b).

The first step is to create a sequence of suitable pulses, each related to a particular frequency of the FM signal, in order to evaluate the TOF. For simplicity, the FM_2 echo component and the related neural network will be considered. The FM_2 signal is a down-chirp from 65 kHz to 49 kHz with a duration of about 6 ms, from which a sequence of suitable pulses is created to activate the artificial neural network.

In the electronic system the pulse sequence related to the spectral components is obtained by filtering and then rectifying the FM_n (n=2…4) signals. Finally the signal is again filtered at low frequency to extract the envelope shown in Figure 13.

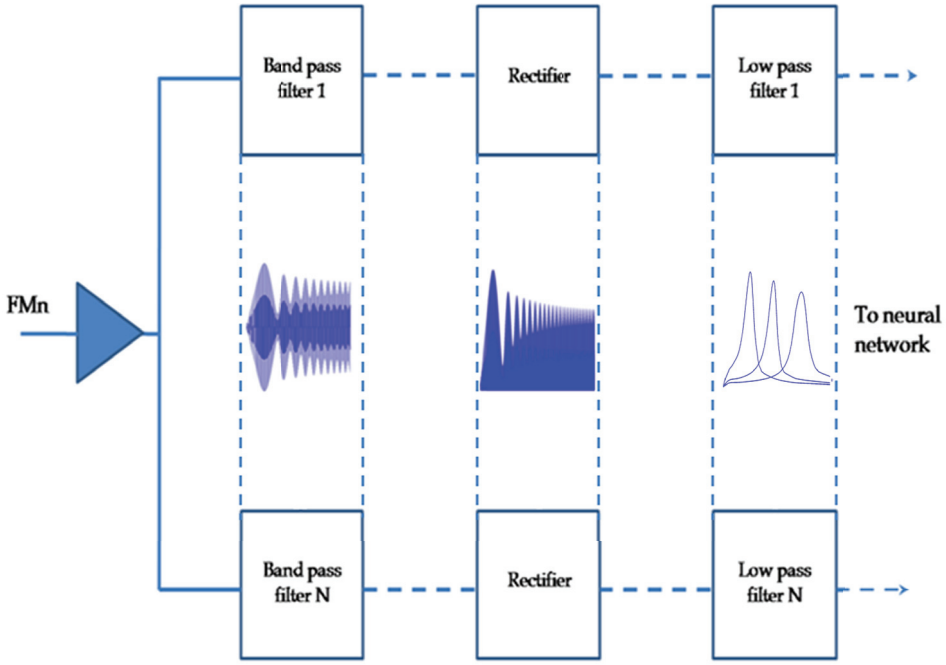


Fig. 13. Schematic simulation of cochlea signal conditioning

These pulse signals are sent in parallel to the neural network which compares the first component PFM_1 with each one of the other three EFM_2, EFM_3, EFM_4 in three different neural structures: PFM_1-EFM_2, PFM_1-EFM_3 and PFM_1-EFM_4.

Similarly PFM_1 is converted in a sequence of pulses according to a time-frequency correspondence. In fact, when both PFM and EFM signals reach the neural network as a pulse sequence, frequency losses sense since it is related to the particular delayed pulse. According to the Suga model, neurons A and C respond to the stimulus with action potentials, while in our electronic system voltage pulses are sent, from neurons A and C through neurons B and D, in the afferent ways, to the time axis.

In Figure 14 one can see the neural network learned and simulated in Matlab in which only three neurons A (C) and four FM-FM neurons along the time axis are considered, for simplicity's sake. The A neurons, which receive the output signal from the block diagram shown in Figure 13, are implemented by using a multilayer perceptron structure trained with a back propagation algorithm. It reduces the envelope duration around its peak value (see Figure 15) in order to improve the cross-correlation analysis performed by the FM-FM neurons.

The neural model offers a possible description in terms of cross-correlation analysis according to signal codification and time of flight detection as in bat biosonar for ranging evaluation.

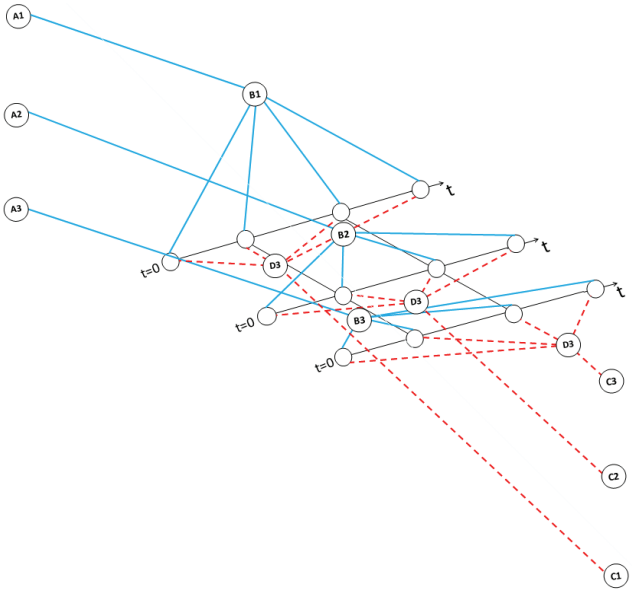


Fig. 14. Portion of a three-level neural network in which each neuron A (or C) receives the corresponding envelope that is sent through neurons B (or D) to FM-FM neurons

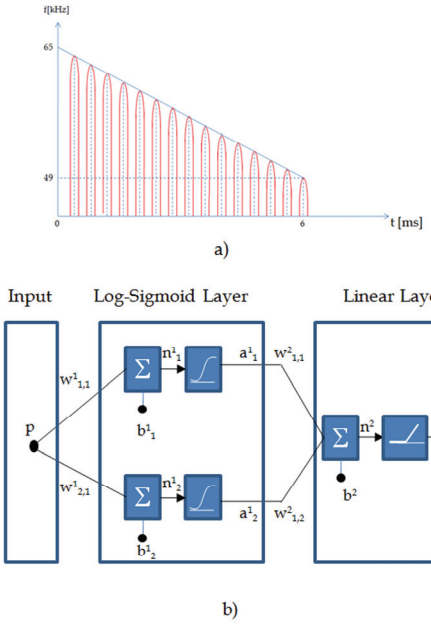


Fig. 15. a) Sequence of 16 pulses, related to a 16 echo envelope, at the output of A neurons. b) Neuron multilayer perceptron implemented in Matlab environment

6. Conclusion and future development

It is our opinion that ferroelectric polymer-based sensors for low frequency ultrasound in air represent the best compromise between versatility and performance.
In effect, the curved PVDF ultrasonic transducer is the only one capable of resonating over a wide frequency range. In fact, the functioning of the majority of standard or custom transducers, based on different technologies, is limited to narrow frequency bands which reduce their use to a restricted field of application. For this reason most research is concerned with signal processing rather than transducer technology. The efficiency of ultrasonic transducers is clearly improved by the ferroelectric polymer technologies. PVDF transducers can adapt work modalities to tasks almost in medium range application in air according to strategies observed in the flight of bats.
Our work shows the possibility of using PVDF transducers to replicate the behaviour of bat bio-sonar despite the fact that only ranging was considered. Future developments must be concerned with the implementation of suitable neural networks for the explication of different tasks as relative to velocity, target size and finer characteristics. All of these problems could be approached in terms both of technology and of neural networking.

7. References

Altringham, J. (1986). *Bats: biology and behavior*. Oxford University Press, New York

Bauer, F. (1986). Method and device for polarizing ferroelectric materials, *U.S. Patent 4,611,260*, USA

Bergman, J.G., McFee, J.H., Crane, G.R. (1971). Pyroelectricity and optical second harmonic generation in polyvinylidene fluoride films, *Applied Physics Letter*, Vol. 18, No. 5, pp. 203-205, 0003-6951

Berlincourt, D. (1981). Piezoelectric ceramics: characteristics and applications, *Journal of the Acoustical Society of America,* Vol. 70, No. 6, pp. 1586-1595, 0001-4966

Bloomfield, P.E., Marcus, M.A. (1988). Production of ferroelectric polymer films, In *Applications of Ferroelectric Polymers*, Wang, T.T., Herbert, J.M., Glass, A.M., Blackie & Son Ltd, Chapman and Hall, New York

Brown, L.F., Carlson, D.L. (1989). Ultrasound transducer models for piezoelectric polymer films, *IEEE Transaction on Ultrasonics, Ferroelectrics and Frequency Control*, Vol. 36, No. 3, pp. 313–318, 0885-3010

Davis, G.T. (1988). Structure, morphology, and models of polymer ferroelectrics, In *Applications of Ferroelectric Polymers*, Wang, T.T., Herbert, J.M., Glass, A.M. Blackie & Son Ltd, Chapman and Hall, New York

De Condillac, E.B. (1754). *Condillac's treatise on the sensations,* Geraldine Carr (trans.), Favil Press, London

Hasegawa, R., Takahashi, Y., Chatani, Y., Tadokoro, H. (1972). Crystal structure of three crystalline forms of poly(vinylidene fluoride), *Polymer Journal*, Vol. 3, pp. 600-610

Hasegawa, R., Kobayaschi, M., Tadokoro, H. (1972). Molecular conformation and packing of poly(vinylidene fluoride). Stability of three crystalline forms and the effect of high pressure, *Polymer Journal*, vol. 3, No.5, pp. 591-599

Hunt, J.W., Arditi, M., Foster, F.S. (1983). Ultrasound transducers for pulse echo medical imaging, *IEEE Transaction on Biomedical Engineering*, Vol. BME-30, No. 8, pp. 453-481, 0018-9294

Jona, F, Shirane, G. (1962). *Ferroelectric crystals*, Pergamon Press, New York

Fiorillo, A.S. (2000). Noise analysis in air-coupled PVDF ultrasonic sensors, *IEEE Transaction on Ultrasonics, Ferroelectrics and Frequency Control*, Vol. 47, No.6, pp. 1432-1437, 0085-3010

Fiorillo, A.S. (1996). Ultrasound transducer with low synthetic quality factor, *Applied Physic Letters*, Vol. 68, No. 2, pp. 164-166, 0003-6951

Fiorillo, A.S., Design and characterization of a PVDF ultrasonic range sensor, *IEEE Transaction on Ultrasonics Ferroelectrics and Frequency Control*, Vol. 39, No. 6, pp 688-692, 0085-3010

Fiorillo, A.S., Van der Spiegel, J., Esmail-Zandi, D., Bloomfield, P.E. (1990). A P(VDF/ TrFE) based integrated ultrasonic transducer, *Sensors and Actuators A: Physical*, Vol. 22, No.1-3, pp. 719-725, 0924-4247

Fiorillo, A.S., Lamonaca, F., Pullano, S.A. (2010). PVDF based sonar for a remote web system to control mobile robots, *Sensors & Transducers Journal*, Vol. 8, Special Issue, pp. 65-73, 1726-5479

Hazas, M., Hopper, H. (2006). Broadband ultrasonic location systems for improve indoor positioning, *IEEE transaction on Mobile Computing*, Vol. 5, No. 5, pp. 536-547, 1536-1233

Lewin, P.A., De Reggi, A.S. (1988). Short range applications, In *Applications of Ferroelectric Polymers*, Wang, T.T., Herbert, J.M., Glass, A.M. Blackie & Son Ltd, Chapman and Hall, New York

Lovinger, A.J. (1983). Ferroelectric polymers, *Science*, Vol. 220, No. 4602, pp. 1115-1121

Lovinger, A.J. (1982). Developments in crystalline polymers, *Applied Science*, Vol. 1, No.5

Mason, W.P. (1981). Piezoelectricity, its history and applications, *Journal of the Acoustical Society of America, Vol. 70*, No. 6, pp. 1561-1566

Mason, W.P. (1964). *Piezoelectric crystals and their applications to ultrasonic*, Van Nostrand Company, Inc. 4th ed., New York

Sessler, G.M. (1981). Piezoelectricity in polyvinylidenefluoride, *Journal of the Acoustical Society of America,* Vol. 70, No. 6, pp. 1596–1608

Swartz, R.G., Plummer, J.D., Integrated silicon-PVF2 acoustic transducer arrays, *IEEE Transaction on Electron Devices*, Vol. 26, No. 12, pp 1921-1931, 0018-9383

Suga, N. (1990). Cortical computational maps for auditory imaging, *Neural Networks*, Vol.3, No. 1, pp.3-21, 0893-6080

Toda, M., Tosima, S. (1999). Theory of curved clamped PVDF acoustic transducers, *Proceeding of IEEE Ultrasonic Symposium*, 1051-0117, Caesars Tahoe, October

Wang, H., Toda, M. (1999). Curved PVDF airborne transducer, *IEEE Transaction on Ultrasonics Ferroelectrics and Frequency Control*, Vol. 46, No. 6, pp. 1375–1386, 0885-3010

Yamaka, E., Teranishi, A. (1977). Pyroelectric Vidicon Tube with PVF, Film and Its Application, *Proceeding of the 1st Meeting on Ferroelectric Materials and Their Applications*, Kyoto, November

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Ferroelectric Materials for Small-Scale Energy Harvesting Devices and Green Energy Products

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1. Introduction

Portable electronic devices and autonomous systems experienced a strong development over the last few years, thanks to progresses in microelectronics and ultralow-power circuits, as well as because of an increasing demand in autonomous and "left-behind" sensors from various industrial fields (for instance aeronautic, civil engineering, biomedical engineering, home automation). Until now, such devices have been powered using primary batteries. However, such a solution is often inadequate as batteries raise maintenance issues because of their limited lifespan (typically one year under normal conditions - Roundy, Wright and Rabaey (2003)) and complex recycling process (leading to environmental problems). In order to tackle these drawbacks, many efforts have been placed over the last decade on systems able to harvest electrical energy from their close environment (Krikke, 2005; Paradiso and Starner, 2005). Many sources are available for power scavenging, such as solar, magnetic, mechanical (vibrations) or thermal (Hudak and Amatucci, 2008). In order to power up small-scale devices, a particular attention has been placed on the last two sources (Anton and Sodano, 2007; Beeby, Tudor and White, 2006; Jia and Liu, 2009; Vullers *et al.*, 2009), as they are commonly available in many environments and because the conversion materials can be easily integrated within the host structure.

The purpose of this chapter is to give a comprehensive view and analysis of small-scale energy harvesting systems using ferroelectric materials, with a special focus on piezoelectric and pyroelectric devices for vibration and thermal energy scavenging systems, respectively. As the energy that can be provided from microgenerators is still limited to the range of tens of microwatts to a few milliwatts, a careful attention has to be placed on the design of the harvester. In particular, backward couplings that may occur between each conversion and energy transfer stages require a global optimization rather than an individual design of each block.

The chapter is organized as follows. Section 2 aims at presenting energy sources and conversion materials that will be considered in this study, as well as basic models for the considered conversion devices. Then section 3 will give a general view of a typical microgenerator, emphasizing the energy conversion chain and issues for optimizing the energy flow. Sections 4 and 5 will focus on two important energy conversion stages (energy conversion and extraction), highlighting general optimization possibilities to get an efficient energy harvester. Implementation issues for realistic applications will then be discussed in

Section 6. Section 7 will present some application examples to self-powered systems. Section 8 will finally briefly conclude the chapter.

2. Energy sources and modeling

Two conversion effects of ferroelectric materials will be considered through this chapter: piezoelectricity, which consists of converting input mechanical energy into electricity, and pyroelectricity, allowing harvesting energy from temperature variations. Therefore, two energy sources will be considered in this study: mechanical energy and thermal energy. The constitutive equations for piezoelectric materials are given by:

$$\begin{cases} \mathrm{d}T = c^E \mathrm{d}S - e^t \mathrm{d}E \\ \mathrm{d}D = \epsilon^S \mathrm{d}E + e\mathrm{d}S \end{cases}, \tag{1}$$

where D, E, S and T respectively refer to electric displacement, electric field, strain and stress tensors. c^E, e and ϵ^S stand for elastic rigidity of the material, piezoelectric coefficient and electric permittivity under constant strain. Finally, d and ^{t} represent the differentiation and transpose operators respectively. In the case of pyroelectric devices, the equations yield:

$$\begin{cases} \mathrm{d}\sigma = p\mathrm{d}E + c\frac{\mathrm{d}\theta}{\theta_0} \\ \mathrm{d}D = \epsilon^\theta \mathrm{d}E + p\mathrm{d}\theta \end{cases}, \tag{2}$$

with θ and θ_0 the temperature and mean temperature, σ the entropy of the system, p the pyroelectric coefficient, c the heat capacitance and ϵ^θ the electric permittivity under constant temperature.

This allows the derivation of energy densities that may be typically obtained. Table 1 gives the comparison of the electrostatic energy density of the two devices for a typical solicitation. It can be seen that the two materials feature relatively close energy density values. This can be explained by the fact that, although piezoelectric coupling is generally much higher than pyroelectric coupling, the input mechanical energy is usually much less than the energy generated by temperature variation. Therefore, the global energy, given by the product of input energy by conversion abilities, is similar for the two materials. Nevertheless, as mechanical frequencies are typically much higher than thermal frequencies, the output power of piezoelectric-based microgenerators is greater than devices using pyroelectric materials (Guyomar *et al.*, 2009; Lallart, 2010a).

Moreover, because of their higher coupling coefficients, extracting energy from piezoelectric elements can affect the mechanical behavior of the system, while the coupling of pyroelectric devices is small enough to neglect the backward coupling (*i.e.*, only the second equation of Eq. (2) can be taken into account).

The model of a global structure can also be obtained from the local constitutive equations Eqs. (1) and (2). In the case of a piezoelectric element (possibly bonded on a structure under

	Piezoelectric	Pyroelectric
Material	NAVY-III type ceramic	PVDF film
Conversion coefficient	$e_{33} = 12.79$ C.m^{-2}	$p = -24e - 6$ C.m^{-2}.K^{-1}
Relative permittivity	$\epsilon_{33}^S/\epsilon_0 = 668$	$\epsilon_{33}^\theta/\epsilon_0 = 12$
Typical input variation	$\Delta S = 10$ μm.m^{-1}	$\Delta\theta = 1$ K
Electrostatic energy density	$(W_{el})_{piezo} = 1.4$ μJ.cm^{-3}	$(W_{el})_{pyro} = 2.7$ μJ.cm^{-3}

Table 1. Energy densities for typical piezoelectric and pyroelectric materials

flexural solicitation), it can be shown that the system may be modeled around one of its resonance frequencies by an electromechanically coupled spring-mass-damper system (Badel *et al.*, 2007; Erturk and Inman, 2008):

$$\begin{cases} M\ddot{u} + C\dot{u} + K_E = F - \alpha V \\ I = \alpha_u \dot{u} - C_0 \dot{V} \end{cases}, \tag{3}$$

where u, F, V and I refer to the displacement (at a particular position of the structure), applied force, piezovoltage and current flowing out of the active material. M, C and K_E denote the dynamic mass, structural damping coefficient and short-circuit stiffness of the system, while α_u and C_0 are given as the force factor and clamped capacitance of the piezoelectric insert.
In the case of pyroelectric energy harvesting, it has previously been stated that the low coupling coefficient permits neglecting the backward coupling. Hence, only the electrical equation is necessary, leading to the macroscopic equation (Guyomar *et al.*, 2009; Lallart, 2010a):

$$I = \alpha_\theta \dot{\theta} - C_0 \dot{V}, \tag{4}$$

with α_θ the pyroelectric factor.

3. Overview of a microgenerator

The principles of an energy harvester lie in several energy conversion and transfer stages to convert the input energy into electrical energy supplied to a load. Basically, four intermediate stages appear between the energy source and the device to power up (Figure 1):

1. Conversion of the raw input energy into effective energy that can be transferred to the active material.
2. Conversion of the energy available in the material into electrical energy.
3. Extraction of the electrical energy available on the material.
4. Storage of the extracted energy.

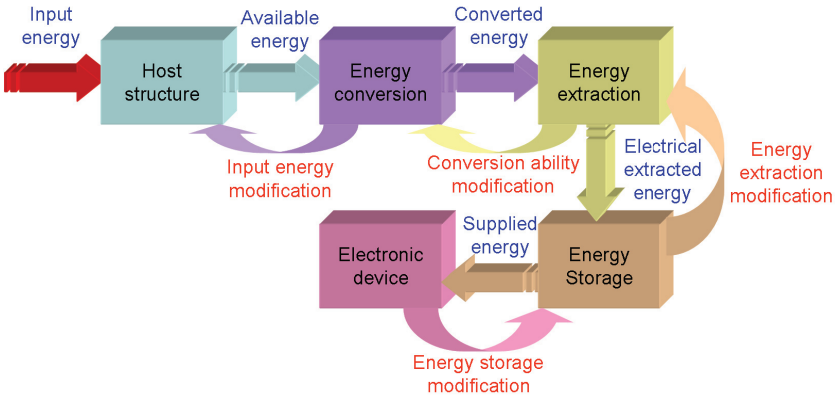


Fig. 1. General energy harvesting chain

However, the energy transfer is not unidirectional. There exist backward couplings that alter the behavior of the previous stage (Figure 1). Therefore, because of these backward couplings, the design of an efficient energy harvester should take the whole system into account. In particular, three main issues have to be considered to dispose of an effective microgenerator:

- Maximization of the energy that enters into the host structure.
- Enhancement of the conversion abilities of the material.
- Optimization of the energy transfer.

3.1 Piezoelectric system

When considering vibration energy harvesting using the piezoelectric effect, two cases can be considered. Either the piezoelectric element is directly bonded on the structure (Figure 2(a)), yielding an open-circuit piezovoltage that is a direct image of the strain and stress within the host structure, or an additional mechanical system is used (Figure 2(b)), allowing an easier maintenance but requiring a fine tuning of the resonance frequency so that it matches one of the mode of the host structure[1]. In all the cases however, the system is operating under dynamic mode in order to dispose of a significant amount of mechanical energy (Keawboonchuay and Engel, 2003).

In the case of direct coupling the energy provided by the input force is first converted into mechanical energy through the host structure, and then to electrostatic energy by the piezoelectric element, while when using indirect coupling an additional mechanical to mechanical energy conversion stage appears (a part of the energy in the host structure is transferred to the additional mechanical system).

The previous design criteria when using piezo-based microgenerators therefore consist of:

- Properly positioning the piezoelement near maximum strain/stress locations (for direct coupling) or maximum acceleration areas (for indirect coupling) and adapting the additional structure to the host structure in the case of seismic coupling.
- Using piezoelectric elements featuring high coupling coefficients and/or using artificial enhancement of the global coupling factor.
- Adapting the load seen by the piezoelectric element.

Obviously, the interdependence of the conversion stages necessitates a global approach rather than an individual optimization. A typical example is the damping effect generated by the harvesting process (Lesieutre, Ottman and Hofmann, 2003): as a significant part of the mechanical energy is converted into electricity, the former decreases, limiting the vibrations of the structure and thus the output electrical power.

(a) Direct coupling (b) Indirect (seismic) coupling

Fig. 2. Typical configurations for vibration energy harvesting using piezoelectric elements

[1] In the case of seismic coupling multimodal energy harvesting is therefore delicate.

Generally, the structure optimization consists of allowing a large amount of energy to enter in the piezoelectric element (which can be obtained by using a proper geometry - Zhu, Tudor and Beeby (2010)) and ensuring a wide frequency range operation, hence allowing energy entering whatever the force frequency is. This can be achieved by using variable resonance frequency (Challa *et al.*, 2008; Lallart, Anton and Inman, 2010b) or using nonlinear structures (Andò *et al.*, 2010; Blystad and Halvorsen, 2010a; Erturk, Hoffmann and Inman, 2009; Soliman *et al.*, 2008). Another commonly adopted solution is to use several cantilevers with different lengths (Shahruz, 2006), which however decreases the power density. The optimization of the last two items will be exposed in Sections 4 and 5.

3.2 Pyroelectric system

The case of pyroelectric energy harvesting consists of extracting energy of time-variable heat trough the thermal capacitance of the active material (Figure 3). The optimization of the input energy lies in the trade-off in the heat capacitance value, as energy should enter easily (low heat capacitance value and high thermal conductivity) and amount of available energy (high heat capacitance value).
For the conversion stage, the design is easier than in the case of piezoelectric elements, as the backward coupling can be neglected in almost all pyroelectric systems. In addition, as pyroelectric effect principles are close to those of the piezoelectric effect, the conversion enhancement and transfer optimization are similar to the case of piezo-based devices, as it will be explained in Sections 4 and 5.

4. Conversion improvement

The purpose of this section is to expose possibilities for improving the energy conversion. To introduce this concept, it is proposed to consider a piezoelectric-based system. From the equation of motion of the simple spring-mass-damper model (Eq. (3)), the energy analysis over a time period $[t_0; t_0 + T]$ is obtained by integrating in the time-domain the product of the equation by the velocity:

$$\frac{1}{2}M\left[\dot{u}^2\right]_{t_0}^{t_0+T} + \frac{1}{2}K_E\left[u^2\right]_{t_0}^{t_0+T} + C\int_{t_0}^{t_0+T}(\dot{u})^2\,dt + \alpha_u\int_{t_0}^{t_0+T}V\dot{u}dt = \int_{t_0}^{t_0+T}F\dot{u}dt, \tag{5}$$

where all the corresponding energies are given in Table 2. Therefore it can be seen that the converted energy depends on the force factor α_u and on the time integral of the product of the voltage by the speed:

$$W_{conv}|_{piezo} = \alpha_u\int_{t_0}^{t_0+T}V\dot{u}dt. \tag{6}$$

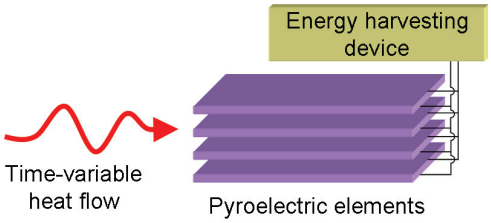


Fig. 3. Typical configuration for thermal energy harvesting using pyroelectric elements

Term	Meaning
$\frac{1}{2}M\left[\dot{u}^2\right]_{t_0}^{t_0+T}$	Kinetic energy
$\frac{1}{2}K_E\left[u^2\right]_{t_0}^{t_0+T}$	Potential energy
$C\int_{t_0}^{t_0+T}(\dot{u})^2\,dt$	Dissipated energy
$\alpha_u\int_{t_0}^{t_0+T}V\dot{u}dt$	Converted energy
$\int_{t_0}^{t_0+T}F\dot{u}dt$	Provided energy

Table 2. Definition of the energies in the case of piezoelectric energy harvesting

Such an analysis can obviously be applied to pyroelectric conversion, yielding the amount of converted energy:

$$W_{conv}|_{pyro} = \alpha_\theta \int_{t_0}^{t_0+T} V\dot{\theta}dt \tag{7}$$

Hence, in order to enhance the conversion abilities of the system, three ways can be explored:

- Increase α_u (for vibration energy harvesting) or α_θ (for thermal energy harvesting).
- Increase the voltage.
- Decrease the time shift between voltage and speed (or temperature variation rate).

Usually, the first point corresponds to the use of piezoelectric materials with higher intrinsic coupling coefficient (Rakbamrung *et al.*, 2010). This has been done recently through the use of single crystal devices (Khodayari *et al.*, 2009; Park and Hackenberger, 2002; Sun *et al.*, 2009), which typically allows increasing the harvested power by a factor of 20 (Badel *et al.*, 2006). However, single crystals are difficult to obtain, and no industrial process has been achieved, compromising the design of low-cost microgenerators using such materials.
In order to enhance the harvesting abilities, a nonlinear approach has been proposed that allows an artificial increase of the global electromechanical coupling coefficient (Guyomar *et al.*, 2005; Lefeuvre *et al.*, 2006; Makihara, Onoda and Miyakawa, 2006; Qiu *et al.*, 2009; Shu, Lien and Wu, 2007). This process consists of quickly inverting the piezoelectric voltage when the displacement or temperature reaches a maximum or a minimum value (or equivalently when the velocity cancels), as shown in Figure 4. Thanks to the dielectric behavior of piezoelectric and pyroelectric materials, the voltage is continuous. Hence, the inversion process allows a cumulative voltage increase effect, as well as an additional piecewise constant voltage that is proportional to the sign of the velocity, allowing a magnification of the energy conversion using both the voltage increase and the reduction of the time shift between voltage and velocity. Practically, the inversion of the voltage is obtained by intermittently connecting the active material to an inductor L (Figure 5), shaping a resonant network which permits the voltage inversion if the switch SW is open for half an electrical oscillation period. Nevertheless, the losses in this switching circuit lead to an imperfect inversion characterized by the inversion factor γ (corresponding to the ratio between absolute voltages after and before the inversion), which is comprised between 0 (no inversion - voltage cancellation) and 1 (perfect inversion).
In the framework of energy harvesting, the switching element can be placed either in parallel or in series with the classical energy harvesting circuit (which consists of connecting the material to a diode rectifier bridge and a smoothing capacitor C_s as shown in Figure 6(a)), respectively leading to the principles of the parallel *Synchronized Switch Harvesting on Inductor*

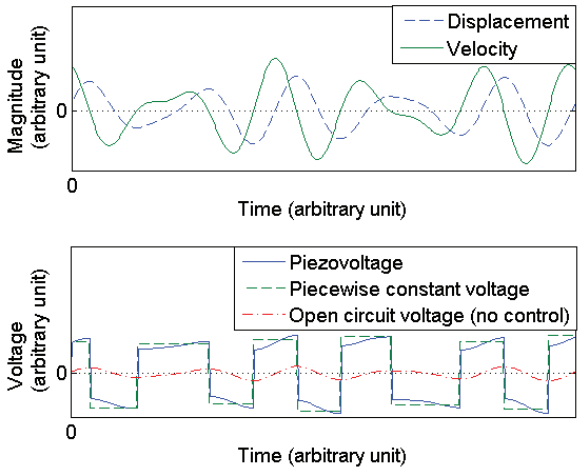


Fig. 4. Nonlinear treatment principles

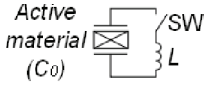
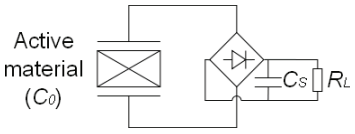
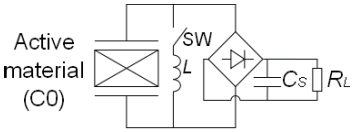


Fig. 5. Practical implementation of the voltage inversion technique

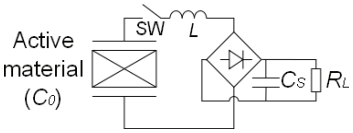
(parallel SSHI - Figure 6(b) - Guyomar *et al.* (2005)) and series *Synchronized Switch Harvesting on Inductor* (series SSHI - Figure 6(c) - Lefeuvre *et al.* (2006); Taylor *et al.* (2001)). Such an approach typically allows a gain of 10 using classical components compared to the classical technique when considering constant displacement magnitude. Harvested energies as a function of the systems parameters (with f_0 the vibration frequency, X_M the displacement or temperature variation magnitude and R_L the equivalent connected load) are listed in Table 3.
However, backward coupling influences the mechanical behavior of the host structure (more particularly by introducing a damping effect) when using piezoelectric energy harvesting at the resonance frequency. In this case, it is possible to get the displacement magnitude u_M from the mechanical energy analysis of the system, leading to the normalized harvested



(a) Classical



(b) Parallel SSHI



(c) Series SSHI

Fig. 6. Energy harvesting circuits

Technique	Harvested energy	Maximal harvested energy	Gain ($\gamma = 0.8$)
Standard	$\frac{(4\alpha f_0)^2 R_L}{(1+4R_L C_0 f_0)^2} {X_M}^2$	$\frac{\alpha^2}{C_0} f_0 {X_M}^2$	–
Parallel SSHI	$\frac{(4\alpha f_0)^2 R_L}{[1+2(1-\gamma)R_L C_0 f_0]^2} {X_M}^2$	$\frac{2}{1-\gamma}\frac{\alpha^2}{C_0} f_0 {X_M}^2$	10
Series SSHI	$\frac{[4(1+\gamma)\alpha f_0]^2 R_L}{[(1-\gamma)+4(1+\gamma)R_L C_0 f_0]^2} {X_M}^2$	$\frac{1-\gamma}{1-\gamma}\frac{\alpha^2}{C_0} f_0 {X_M}^2$	9

Table 3. Harvested energies for classical and SSHI techniques and gain under constant displacement magnitude

powers depicted in Figure 7. To make this chart as independent as possible from the system parameters, the power has been normalized with respect to the maximal harvested power in the standard case when taking into account the damping effect:

$$P_{lim} = \frac{{F_M}^2}{8C}, \tag{8}$$

with F_M the driving force magnitude. The x-axis of Figure 7 corresponds to the figure of merit given by the product of the squared global coupling coefficient k^2 (reflecting the amount of energy that can be converted) by the mechanical quality factor Q_M (giving an image of the effective available energy). This figure shows that the standard and SSHI techniques feature the same power limit, but the nonlinear approaches permit harvesting the same amount of energy than the classical scheme for much lower values of $k^2 Q_M$, meaning that much less volume of active materials is required. Figure 7 also shows that the series SSHI performance is very close to the parallel SSHI. It can be noted that these nonlinear approaches also permit increasing the bandwidth of the microgenerator (Lallart *et al.*, 2010c). Losses in the inductance that limit the power increase can also be controlled using proper approaches, such as smoother inversion (Lallart *et al.*, 2010d), PWM actuation that insures a perfect inversion[2] (Liu *et al.*, 2009) or by ensuring that the inversion losses are always less than the converted energy over a given time period (Guyomar and Lallart, 2011).

Finally, another way to enhance the conversion abilities is to consider a bidirectional energy flow from the source to the storage stage (Lallart and Guyomar, 2010e). This approach permits beneficiating of a particular "energy resonance" effect as the converted energy equals the

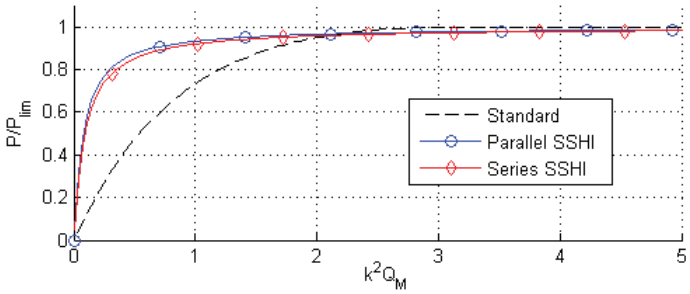


Fig. 7. Normalized harvested powers under constant force magnitude at the resonance frequency

[2] In this case, driving losses may however compromise the energy balance.

converted energy without providing initial energy (from the storage stage) plus twice the cross-product of the initial voltage V_0 times the voltage generated by the active material:

$$W_{conv}|_{bidir} = \frac{1}{2}C_0\left(\frac{\alpha}{C_0}X_M + V_0\right)^2 - \frac{1}{2}C_0{V_0}^2 = \frac{1}{2}\left[\frac{\alpha^2}{C_0}{X_M}^2 + 2\alpha V_0 X_M\right]. \quad (9)$$

Hence, as the harvested energy increases, the initial provided energy during the beginning of a new cycle increases as well, allowing harvesting more energy, and therefore closing the "energy resonance" loop. This approach permits a typical harvested energy gain up to 40 under constant displacement magnitude (or constant temperature variation magnitude) as well as bypassing the power limit when considering the damping effect.

It can also be noticed that instead of adding external nonlinearities, Guyomar, Pruvost and Sebald (2008); Khodayari *et al.* (2009); Zhu *et al.* (2009) have shown that the energy harvesting performance may be also enhanced by using the intrinsic nonlinear behaviors of pyroelectric materials, such as ferroelectric↔ferroelectric or ferroelectric↔paraelectric phase transitions.

5. Energy transfer optimization

The next stage in the energy conversion chain lies in the energy transfer from the active material to the storage stage. As the amount of energy provided to the electronic device may alter the energy conversion process (which can be seen from the load-dependent powers in Table 3 and in Figure 8), additional interfaces have to be included so that the energy extracted from the active material is maximum. This section proposes to expose two possibilities to ensure a harvested energy independent from the connected load by:

- Ensuring that the active material sees the optimal load.
- Decoupling the extraction and storage stage through a nonlinear approach.

The simplest way for ensuring that the load seen by the piezoelectric or pyroelectric material equals the optimal one that maximizes the harvested power consists of adding a converter between the active element and the extraction stage (Han *et al.*, 2004; Lallart and Inman,

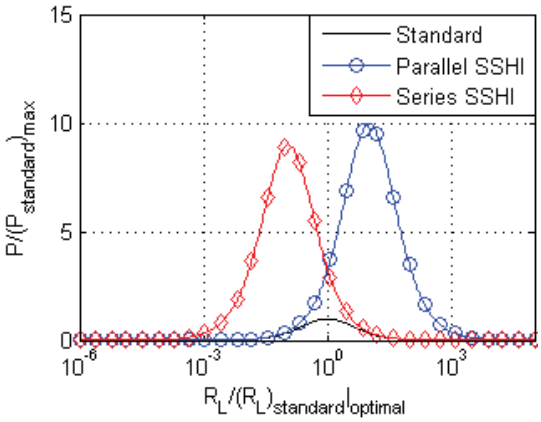


Fig. 8. Normalized harvested powers under constant displacement magnitude (or constant temperature variation magnitude) as a function of the load (normalized with respect to the optimal load in the standard case)

2010f; Lefeuvre *et al.*, 2007a; Ottman *et al.*, 2002; Ottman, Hofmann and Lesieutre, 2003). The converter should operate in discontinuous mode in order to present a constant (or almost constant) impedance to the piezoelectric element. Usually, the converter parameter (inductance L, switching frequency f_{sw} and duty cycle δ) should also be tuned so that its input impedance is close to the optimal load that maximizes the extracted energy (Table 4)[3], although an automatic detection of the optimal operating point can be done (Lallart and Inman, 2010f; Ottman *et al.*, 2002).

Another approach for ensuring a harvested energy independent from the load consists of slightly modifying the previously exposed nonlinear techniques. In particular, if the switching time period is reduced so that it stops when the voltage across the active material is zero, all the electrostatic energy available on the material is transferred to the inductance (under magnetic form). If this energy can then be transferred to the load, there would not be any direct connection between the load and the piezoelectric or pyroelectric material, thus allowing a decoupling between the energy extraction stage and the energy storage stage. Such a technique, called *Synchronous Electric Charge Extraction* (Lefeuvre *et al.*, 2005; 2006), is depicted in Figure 9. The SECE approach also permits an enhancement of the conversion thanks to a voltage increase and a reduction of the time shift between voltage and velocity, and allows a typical energy gain of 3.5 compared to the maximal harvested energy in the standard case under constant displacement magnitude.

Nevertheless, the SECE techniques does not allow controlling the trade-off between extracted energy and conversion improvement, as all the energy on the active material is extracted. The principles of the technique may be enhanced by combining the series SSHI approach with the SECE, leading to the DSSH technique (Lallart *et al.*, 2008a). This scheme, depicted in Figure 10, consists in first extracting a part of the electrostatic energy on the piezoelectric or pyroelectric material on an intermediate capacitor C_{int}, while the remaining energy is used to perform the voltage inversion leading to the conversion magnification. Then the energy available on the intermediate capacitor is transferred to the load in the same way than the SECE. Hence, through the ratio between the active element capacitance and intermediate capacitance, it is possible to finely control the trade-off between extracted energy and conversion enhancement, allowing a typical harvested energy 7.5 higher than the maximal harvested energy in the

Type	Impedance	Efficiency
Step-down (Ottman, Hofmann and Lesieutre, 2003)	$\left(\frac{2Lf_{sw}}{\delta^2}\right)\left(\frac{1}{1-\frac{V_{out}}{V_{in}}}\right)$	65%
Buck-boost (Lefeuvre *et al.*, 2007a)	$\left(\frac{2Lf_{sw}}{\delta^2}\right)$	75%

Table 4. Impedance matching systems (V_{out} and V_{in} refer to output and input voltages)

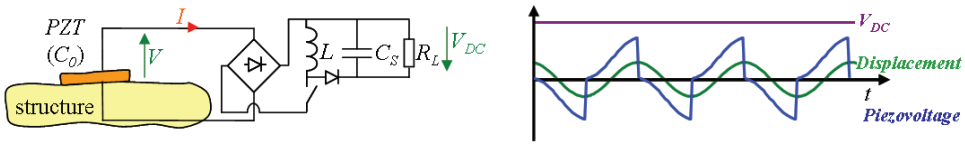


Fig. 9. SECE technique

[3] As the optimal load depends on the frequency, broadband energy harvesting is quite delicate for these architectures.

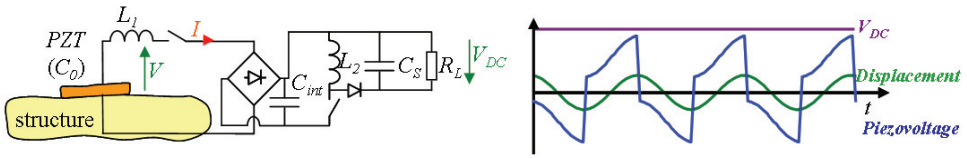


Fig. 10. DSSH technique

standard case under constant displacement magnitude or constant temperature variation magnitude and independent from the connected load. The SECE and DSSH techniques have also the advantage of being able to harvest energy even for low load values, while in the case of low frequency (typical for temperature variation), the optimal load for the standard and SSHI approaches would be very large.

When taking into account the damping effect caused by the backward coupling in the case of mechanical energy harvesting using piezoelectric principles, the harvested energy using the SECE and DSSH techniques is given in Table 5 and depicted in Figure 11.

Figure 11 shows the effectiveness of the techniques for allowing a significant power output even for low values of the figure of merit k^2Q_M, especially for the DSSH approach, which permits the same power output than the standard technique with 10 times less active materials. Contrarily to the SECE technique, the DSSH does not present a decreasing power for large values of k^2Q_M as the intermediate capacitor also permits controlling the trade-off between extracted energy and damping effect (or equivalently the backward coupling between energy conversion stage and host structure). It can be noted that, due to the losses in the inductance during the energy transfer process, the power limit is decreased.

Technique	Harvested energy	
SECE	$\gamma_C \frac{2}{\pi} \frac{k^2Q_M}{\left(1+\frac{4}{\pi}k^2Q_M\right)^2} \frac{{F_M}^2}{C}$	
DSSH[4]	$\gamma_C \frac{2\pi k^2Q_M(1-\gamma)^2}{\left(\pi(1-\gamma)+4k^2Q_M(1+\gamma)\right)^2} \frac{{F_M}^2}{C}$	for $k^2Q_M \leq \frac{4}{\pi}\frac{1-\gamma}{1+\gamma}$
	$\gamma_C \frac{{F_M}^2}{8C}$	for $k^2Q_M \geq \frac{4}{\pi}\frac{1-\gamma}{1+\gamma}$

Table 5. Harvested energies for SECE and DSSH techniques under constant force magnitude (γ_C refers to the energy transfer efficiency)

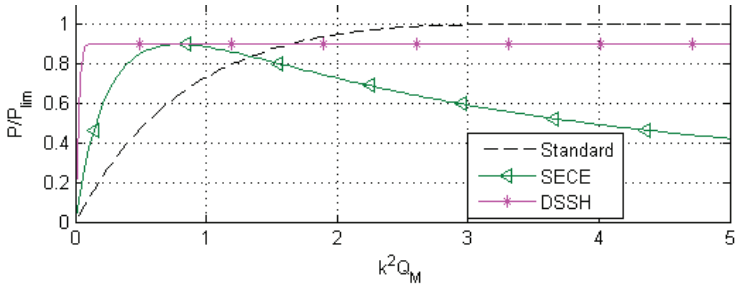


Fig. 11. Harvested energy for the SECE and DSSH techniques ($\gamma_C = 0.9$)

[4] for the optimal intermediate capacitance value

However, this statement has to be weighted by the fact that classical and SSHI approaches require load adaptation stages, whose effectiveness is usually less than 80%. Hence, the power limit of the SECE and DSSH schemes is similar to the one obtained with the other techniques featuring load adaptation stages. Such a statement also applies for constant vibration magnitude or constant temperature variation magnitude case. Finally, it can be noted that the power transfer from the intermediate capacitor to the load can also be controlled by fixing a voltage threshold value, leading to the concept of *Enhanced Synchronized Switch Harvesting* (ESSH) described by Shen *et al.* (2010).

6. Implementation considerations

Now the general principles of energy harvesting exposed, it is proposed in this section to discuss about their implementation for the design of realistic self-powered devices.
The first issue that may arise for the use of nonlinear techniques is the control of the switching device. Actually, the minimum and maximum detection can be done by comparing the voltage across the active material with its delayed version. The maximum is then detected when the delayed signal is greater than the original one (Lallart *et al.*, 2008b; Liang and Liao, 2009; Qiu *et al.*, 2009; Richard, Guyomar and Lefeuvre, 2007). The self-powered autonomous switching device based on this principles therefore consumes very little power, typically less than 5% than the electrostatic energy available on the ferroelectric material, therefore not compromising the energy harvesting gain. The implementation of the self-powered switch, depicted in Figure 12, also shows that only typical electronic components are required, allowing an easy integration of the device.
Another point of interest when designing realistic energy harvesters is the incoming solicitation. While sine excitation is usually considered for theoretical analysis, realistic systems would be more likely subjected to random input (Blystad, Halvorsen and Husa, 2010b; Halvorsen, 2008). Although very few studies addressed this problem in the case of nonlinear energy harvesting (Badel *et al.*, 2005; Lallart, Inman and Guyomar, 2010g; Lefeuvre *et al.*, 2007b), it can be stated that load independent techniques (SECE, DSSH and ESSH) would be more suitable under such circumstance, as the optimal load is frequency-dependent for the other approaches.

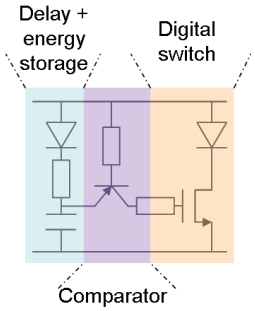


Fig. 12. Principles of the self-powered switch for maximum detection (the minimum detection is simply obtained by reversing the polarity of the system)

Finally, one of the most promising applications of ferroelectric materials used for energy harvesting lies in the MEMS[5] scale. However, when dealing with electroactive microsystems, the output voltage that can be expected is quite low. This may be a serious issue when dealing with energy harvesting as energy harvesting interfaces feature discrete components such as diodes or transistors that present voltage gaps due to their semiconductor nature, hence compromising the operations of the microgenerators. In order to counteract this drawbacks, it is possible to replace the inductance of the series SSHI by a transformer in order to divide the threshold voltage of diodes seen by the piezoelectric element (Garbuio *et al.*, 2009), or to use mechanical rectifiers (Nagasawa *et al.*, 2008).

7. Application examples

In this section two examples of self-powered devices will be exposed, demonstrating the possibility of designing systems powered up by their close environment. However, a careful attention has to be placed on the power management strategy, in order to have a positive energy balance between harvested energy and supplied energy. Some general design rules can be considered for saving energy:

- Use sleep modes as much as possible.
- Optimize components that require the highest energy per operating cycle, rather than devices consuming the highest power. For example, a system that consumes 1 mW for 10 μs (hence necessitating 10 nJ) is therefore less critical than a device requiring 10 μW for 1 s, as the associated energy per cycle of the latter is 10 μJ.
- Re-think the processes to minimize the energy.

7.1 Self-powered accelerometer

The first proposed application example is a self-powered accelerometer. The system is composed by a SSHI energy harvesting device, a microcontroller (for power management, data acquisition and communication management), a low-power accelerometer followed by a filter to obtain the average acceleration and a RF module for data transmission (Figure 13).
When the harvested energy is sufficient (approximately 1 mJ), the microcontroller wakes up and enables the accelerometer as well as the RF transmission module. After a predefined wake-up time, the filtered output signal of the latter is digitized by the microcontroller. The measurement results are then sent by RF transmission together with an identifier. The accelerometer and RF module are finally turned off and the microcontroller enters in sleep

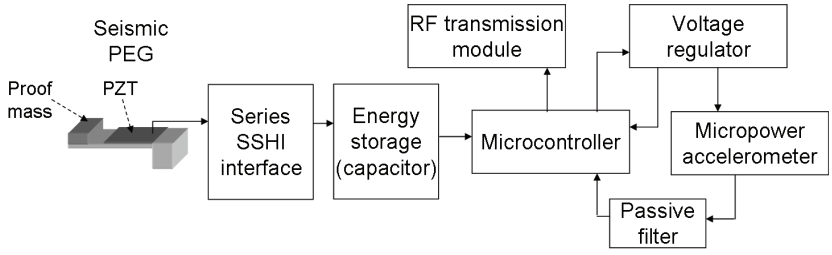


Fig. 13. Architecture of the self-powered accelerometer

[5] *Micro Electro-Mechanical Systems*

mode. If the energy is still sufficient, a new cycle is repeated after a given time period (typically 10 s). The obtained waveforms using this device are depicted in Figure 14.

7.2 Self-powered SHM system

The second autonomous, self-powered wireless system presented in this section lies in a *in-situ* structural condition monitoring system (Figure 15), which consists in analyzing the interaction of an acoustic wave (Lamb wave) with the host structure (Guyomar *et al.*, 2007; Lallart *et al.*, 2008c). The device is made of two self-powered components (Figure 16):

- The *Autonomous Wireless Transmitter* (AWT), which consists in harvesting energy with the SSH module, and when the latter is sufficient, a microcontroller wakes up and applies a pulse voltage on a additional piezoelectric element, which therefore generates the Lamb wave. Then the AWT sends a RF signal containing its identifier for time and space localization before entering into sleep mode for a given time period.
- The *Autonomous Wireless Receiver* (AWR), which also includes a SSHI system. The AWR features a RF listening module which wakes up the system when it senses a RF

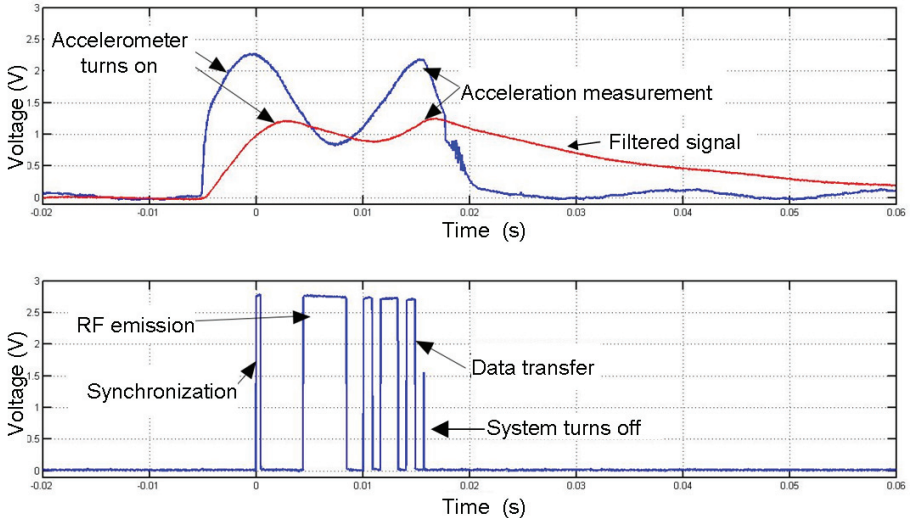


Fig. 14. Waveforms of acceleration measurements and RF comunication

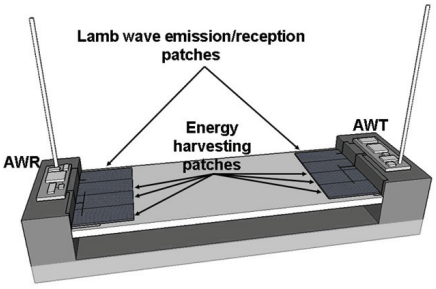
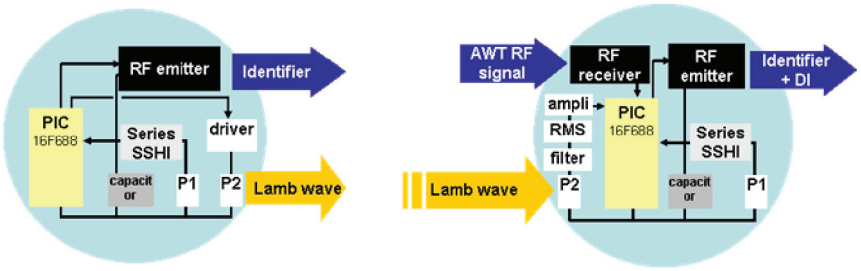


Fig. 15. Self-powered SHM system



(a) AWT (b) AWR

Fig. 16. Structures of the self-powered SHM subsystems

communication incoming from a close AWT. Once woken up, the Lamb wave signature is sensed, amplified, and its RMS value computed. This value is then compared to a reference value (obtained in the pristine case), allowing the estimation of the change in the mechanical structure. The results are then sent by RF transmission together with an identifier. Once these operations terminated, the whole system enters into sleep mode. After a predefined time period, the RF listening module is enabled to detect a new inspection cycle.

In addition, an externally powered base station is used to gather the data. A summary of the communication within the network is depicted in Figure 17 and the energy balance of the system as a function of the stress within the structure is presented in Table 6. The energy consumption estimation for the AWT and AWR are given by:

AWT :

- Microcontroller wake-up: 0.8 mJ
- RF emission: 0.2 mJ
- Lamb wave emission: 0.2 mJ

Total: 1.20 **mJ**

AWR :

- Microcontroller wake-up: 0.8 mJ
- RF listening: 0.6 mJ (average listening time: 3 s)
- Damage Index computation: 0.03 mJ
- RF emission: 0.25 mJ

Total: 1.68 **mJ**

According to Table 6, the system can operate as soon as the stress reaches 2 MPa, which is a realistic stress value in classical structures. It can also be noted that the AWR energy scavenging device features higher global coupling coefficient than the AWT, allowing to harvest more energy in a given time period.

The damage detection estimation has been investigated by adding an artificial damage consisting in a small mass of putty on the structure. Waveforms depicted in Figure 18 demonstrate the ability of the proposed system for quantitatively detecting the change in the structural condition.

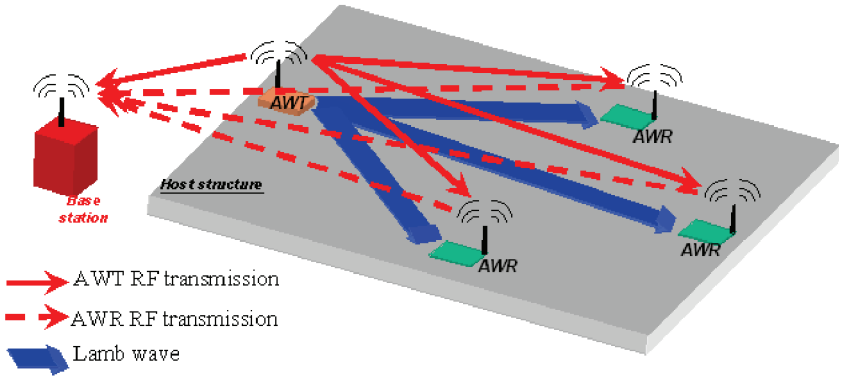


Fig. 17. Communication network for the self-powerd SHM system

Stress (*MPa*)	1.5	1.75	2	2.25	2.5	3	3.5
Harvested energy in 10 s (mJ) for the AWT	0.77	1.05	1.36	1.72	2.13	3.06	4.17
Harvested energy in 10 s (mJ) for the AWR	1.10	1.5	1.96	2.48	3.06	4.41	6.00
Energy balance (mJ) for the AWT	−0.43	−0.15	0.16	0.52	0.93	1.86	2.97
Energy balance (mJ) for the AWR	−0.58	−0.18	0.28	0.80	1.38	2.73	4.32

Table 6. Energy balance for the self-powered wireless SHM device

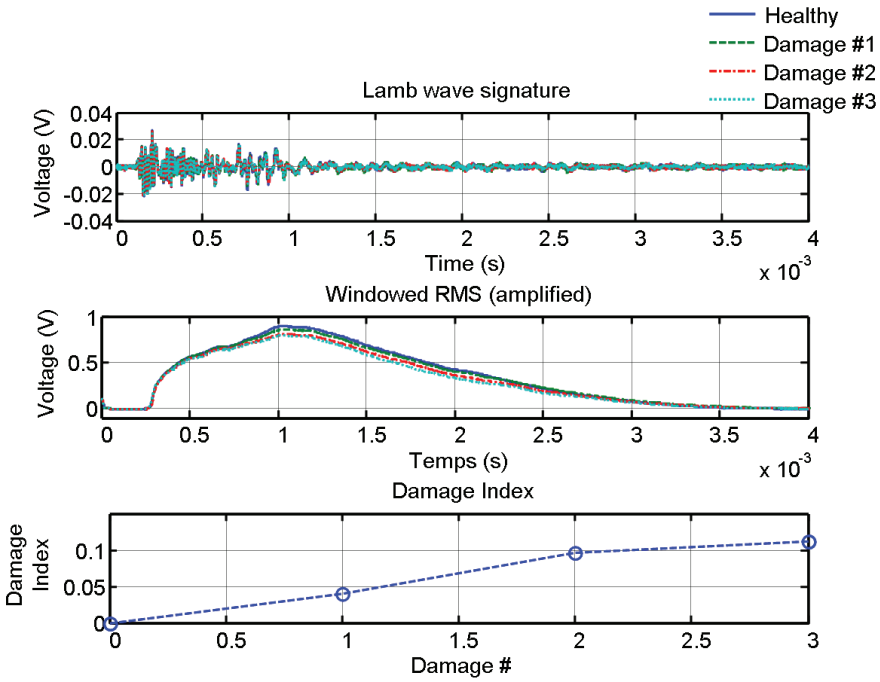


Fig. 18. Results of the self-powered SHM system under artificial damage.

8. Conclusion

This chapter exposed the application of ferroelectric materials to small-scale energy scavenging devices and self-powered systems, with a special focus on vibrations and temperature variations, as ferroelectric devices present high energy densities and promising integration potentials. From the analysis of the global energy transfer chain from the energy source to the device to power up, it has been shown that the design of efficient microgenerators has to be done in a global manner rather than optimizing each block independently, because of backward couplings to may modify the behavior of previous stages. Then several ways for improving the performance of energy harvesters have been explored, showing that the use of nonlinear approaches may significantly increase the energy conversion abilities and/or the independency from the connected device. Fundamental issues such as realistic implementation, performance under real excitation and microscale design have then been discussed. Finally, the possibility of designing truly self-powered wireless systems has been demonstrated through two working application examples, showing that the spreading of devices powered up by energy harvested from their close environment is now only a question of time.

9. References

Andò, B.; Baglio, S.; Trigona, C.; Dumas, N.; Latorre, L. & Nouet, P. (2010). Nonlinear mechanism in MEMS devices for energy harvesting applications. *Smart Mater. Struct.*, Vol. 20, 125020.

Anton, S. R. & Sodano H. A. (2007). A review of power harvesting using piezoelectric materials (2003-2006). *Smart Mater. Struct.*, Vol. 16(3), R1-R21.

Badel, A.; Guyomar, D.; Lefeuvre, E. & Richard, C. (2005). Efficiency Enhancement of a Piezoelectric Energy Harvesting Device in Pulsed Operation by Synchronous Charge Inversion. *J. Intell. Mater. Syst. Struct.*, Vol. 16, 889-901.

Badel, A.; Benayad, A.; Lefeuvre, E.; Lebrun, L.; Richard, C. & Guyomar, D. (2006a). Single Crystals and Nonlinear Process for Outstanding Vibration Powered Electrical Generators. *IEEE Trans. on Ultrason., Ferroelect., Freq. Contr.*, Vol. 53, 673-684.

Badel, A.; Lagache, M.; Guyomar, D.; Lefeuvre, E. & Richard, C. (2007). Finite Element and Simple Lumped Modeling for Flexural Nonlinear Semi-passive Damping. *J. Intell. Mater. Syst. Struct.*, Vol. 18, 727-742.

Beeby, S. P.; M. J.; & White, N. M. (2006). Energy harvesting vibration sources for microsystems applications, *Meas. Sci. Technol.*, Vol. 17, R175-R195.

Blystad, L.-C. J. & Halvorsen, E. (2010a). A piezoelectric energy harvester with a mechanical end stop on one side. *Microsyst. Technol., in press - available online*. DOI: DOI: 10.1007/s00542-010-1163-0.

Blystad, L.-C. J.; Halvorsen, E. & Husa, S. (2010b). Piezoelectric MEMS energy harvesting systems driven by harmonic and random vibrations. *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 57(4), 908-919.

Challa, V. R.; Prasad, M. G.; Shi, Y. & Fisher, F. T. (2008). A vibration energy harvesting device with bidirectional resonance frequency tunability. *Smart Mater. Struct.*, Vol. 17, 015035.

Erturk A. & D. J. Inman (2008). Issues in mathematical modeling of piezoelectric energy harvesters. *Smart Mater. Struct.*, Vol. 17, 065016.

Erturk A.; Hoffmann, J. & D. J. Inman (2010). A piezomagnetoelastic structure for broadband vibration energy harvesting. *Appl. Phys. Lett.*, Vol. 94, 254102.

Garbuio, L.; Lallart, M.; Guyomar, D. & Richard, C. (2009). Mechanical Energy Harvester with Ultra-Low Threshold Rectification Based on SSHI Non-Linear Technique, *IEEE Trans. Indus. Elec.*, Vol. 56(4), 048-1056.

Guyomar, D.; Badel, A.; Lefeuvre, E. & Richard, C. (2005). Towards energy harvesting using active materials and conversion improvement by nonlinear processing, *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 52, 584-595.

Guyomar, D.; Jayet, Y.; Petit, L.; Lefeuvre, E.; Monnier, T.; Richard, C. & Lallart, M. (2007). Synchronized Switch Harvesting applied to Self-Powered Smart Systems : Piezoactive Microgenerators for Autonomous Wireless Transmitters, *Sens. Act. A: Phys.*, Vol. 138, No. 1, 151-160.

Guyomar, D.; Pruvost, S. & Sebald, G. (2008). Energy Harvesting Based on FE-FE Transition in Ferroelectric Single Crystals, *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 55(2), 279-285.

Guyomar, D.; Sébald, G.; Pruvost, S.; Lallart, M.; Khodayari, A. & Richard, C. (2009). Energy Harvesting From Ambient Vibrations and Heat, *J. Intell. Mater. Syst. Struct.*, Vol. 20(5), 609-624.

Guyomar, D. & Lallart, M. (2011). Switching loss reduction in Nonlinear Piezoelectric Conversion under Pulsed Loading, *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 58(3), 494-502.

Halvorsen, E. (2008). Energy Harvesters Driven by Broadband Random Vibrations. *J. Microelectromech. Syst.*, Vol. 17(5), 1061-1071.

Han, J.; Von-Jouanne,A.; Le, T.; Mayaram, K. & Fiez, T. S. (2004). Novel power conditioning circuits for piezoelectric micro power generators. In *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, vol. 3, 1541-1546.

Hudak, N. S. & Amatucci, G. G. (2008). Small-scale energy harvesting through thermoelectric, vibration, and radiofrequency power conversion. *Appl. Phys. Rev.*, Vol. 103, 101301.

Jia, D. & Liu, J (2009). Human power-based energy harvesting strategies for mobile electronic devices. *Front. Energy Power Eng. China*, Vol. 3(1), 27Ú46.

Keawboonchuay , C. & Engel, T. G. (2003). Electrical power generation characteristics of piezoelectric generator under quasi-static and dynamic stress conditions. *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 50, 1377-1382.

Khodayari, A.; Pruvost, S.; Sebald, G.; Guyomar, D. & Mohammadi, S. (2009). Nonlinear Pyroelectric Energy Harvesting from Relaxor Single Crystals. *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 56(4), 693-699.

Krikke, J. (2005). Sunrise for energy harvesting products. *IEEE Pervasive Comput.*, Vol. 4, 4-35.

Lallart, M.; Garbuio, L.; Petit, L.; Richard, C. & Guyomar, D. (2008a) Double Synchronized Switch Harvesting (DSSH) : A New Energy Harvesting Scheme for Efficient Energy Extraction, *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, Vol. 55,(10), 2119-2130.

Lallart, M.; Lefeuvre, E.; Richard, C. & Guyomar, D. (2008b). Self-Powered Circuit for Broadband, Multimodal Piezoelectric Vibration Control. *Sens. Act. A: Phys.*, Vol. 143, No. 2, 277-382, 2008.

Lallart, M.; Guyomar, D.; Jayet, Y.; Petit, L.; Lefeuvre, E.; Monnier, T.; Guy, P. & Richard, C. (2008c). Synchronized Switch Harvesting applied to Selfpowered Smart Systems: Piezoactive Microgenerators for Autonomous Wireless Receiver, *Sens. Act. A: Phys.*, Vol. 147, No. 1, 263-272.

Lallart, M. (2010a). Conversion électroactive et application aux systèmes auto-alimentés[6]. Editions Universitaires Européennes, *in french*. ISBN: 978-613-1-50507-2

Lallart, M.; Anton, S. R. & Inman, D. J. (2010b). Frequency Self-tuning Scheme for Broadband Vibration Energy Harvesting. *J. Intell. Mat. Syst. Struct.*, Vol. 21(9), 897-906 .

Lallart, M.; Guyomar, D.; Richard, C. & Petit, L. (2010c). Nonlinear optimization of acoustic energy harvesting using piezoelectric devices. *J. Acoust. Soc. Am.*, Vol. 128(5), 2739-2748.

Lallart, M.; Garbuio, L; Richard, C. & Guyomar, D. (2010d). High Efficiency, Low-Cost Capacitor Voltage Inverter for Outstanding Performances in Piezoelectric Energy Harvesting, *IEEE Trans. on Ultrason., Ferroelect., Freq. Contr.*, Vol. 57(2), 281-291.

Lallart, M. & Guyomar, D. (2010e). Piezoelectric conversion and energy harvesting enhancement by initial energy injection. Appl. Phys. Lett., Vol. 97, # 014104.

Lallart, M. & Inman, D. J. (2010f). Low-Cost Integrable Tuning-Free Converter for Piezoelectric Energy Harvesting Optimization. *IEEE Trans. Power Electron.*, Vol. 25(7), 1811-1819.

Lallart, M.; Inman, D. J. & Guyomar, D. (2010g). Transient Performance of Energy Harvesting Strategies under Constant Force Magnitude Excitation. *J. Intell. Mater. Syst. Struct.*, Vol 21(13), 1279-1291.

Lefeuvre, E.; Badel, A.; Richard, C. & Guyomar, D. (2005). Piezoelectric energy harvesting device optimization by synchronous electric charge extraction. *J. Intell. Mat. Syst. Struct.*, Vol. 16, No. 10, 865-876.

Lefeuvre, E.; Badel, A.; Richard, C.; Petit, L. & Guyomar, D. (2006). A comparison between several vibration-powered piezoelectric generators for standalone systems, *Sens. Act. A: Phys*, Vol. 126, 405-416.

Lefeuvre, E.; Audigier, D.; Richard, C. & Guyomar, D. (2007a). Buck-boost converter for sensorless power optimization of piezoelectric energy harvester. *IEEE Trans. Power Electron.*, Vol. 22(5), 2018-2025.

Lefeuvre, E.; Badel, A.; Richard, C. & Guyomar, D. (2007b). Energy harvesting using piezoelectric materials: Case of random vibrations. *J. Electrocem.*, Vol. 19(4), 349-355.

Lesieutre, G. A.; G.K. Ottman, G. K. & Hofmann, H. F. (2003). Damping as a result of piezoelectric energy harvesting. *J. Sound Vib.*, Vol. 269(3-5), 991-1001.

Liang, J. R. & Liao, W. H. (2009). An Improved Self-Powered Switching Interface for Piezoelectric Energy Harvesting. In *Proc. of 2009 IEEE International Conference on Information and Automation*, 945-950.

Liu, Y.; Tian, G.; Wang, Y; Lin, J.; Zhang, Q. & Hofmann, H. F. (2009). Active Piezoelectric Energy Harvesting: General Principles and Experimental Demonstration. *J. Intell. Mat. Syst. Struct.*, Vol. 20, 575-585.

Makihara, K.; Onoda, J. & Miyakawa, T. (2006). Low energy dissipation electric circuit for energy harvesting. *Smart Mater. Struct.*, Vol. 15, 1493-1498.

Nagasawa, S.; Suzuki, T.; Takayama, Y.; Tsuji, K. & Kuwano, H. (2008). Mechanical rectifier for micro electric generators. *IEEE 21st International Conference on Micro Electro Mechanical Systems*, Tucson, AZ, USA, January 2008, 992-995.

Ottman, G. K.; Hofmann, H. F.; Bhatt, A. C. & Lesieutre, G. A. (2002). Adaptive Piezoelectric Energy Harvesting Circuit for Wireless Remote Power Supply. *IEEE Trans. Power Electron.*, vol. 17(5), 669-676.

[6] *Electroactive conversion and application to self-powered systems*

Ottman, T. S.; Hofmann, H. F. & Lesieutre, G. A. (2003). Optimized piezoelectric energy harvesting circuit using step-down converter in discontinuous conduction mode. *IEEE Trans. Power Electron.*, Vol. 18(2), 696-703.

Paradiso, J. A. & Starner, T. (2005). Energy scavenging for mobile and wireless electronics. *IEEE Pervasive Computing*, Vol. 4, 18-27.

Park, S.-E. & Hackenberger, W. (2002). High performance single crystals, applications and issues. *Current Opinion in Solid State and Material Science*, Vol. 6, 11-18.

Qiu, J.; Jiang, H.; Ji, H. & Zhu, K. (2009). Comparison between four piezoelectric energy harvesting circuits. *Front. Mech. Eng. China*, Vol. 4(2), 153-159.

Rakbamrung, P.; Lallart, M.; Guyomar, D.; Muensit, N.; Thanachayanont, C.; Lucat, C.; Guiffard, B.; Petit, L. & Sukwisut, P. (2010). Performance Comparison of PZT And PMN-PT Piezoceramics for Vibration Energy Harvesting. *Sens. Act. A: Phys.*, Vol. 163, 493-500.

Richard C.; Guyomar, D. & Lefeuvre, E. (2007). Self-Powered Electronic Breaker With Automatic Switching By Detecting Maxima Or Minima Of Potential Difference Between Its Power Electrodes, *patent # PCT/FR2005/003000*, publication number: WO/2007/063194, 2007.

Roundy, S.; Wright, P. K. & Rabaey, J. (2003). A study of low level vibrations as a power source for wireless sensor nodes. *Comp. Comm.*, Vol. 26, 1131-1144.

Shahruz, S. M. (2006). Design of mechanical band-pass filters for energy scavenging. *J. Sound Vib.*, Vol. 292, 987-998.

Shen, H.; Qiu, J.; Ji, H.; Zhu, K. & Balsi, M. (2010). Enhanced synchronized switch harvesting: a new energy harvesting scheme for efficient energy extraction. *Smart Mater. Struct.*, Vol. 20, 115017.

Shu, Y. C.; Lien, I. C. & Wu, W. J. (2007). An improved analysis of the SSHI interface in piezoelectric energy harvesting. *Smart Mater. Struct.*, Vol. 16, 2253-2264.

Soliman, M. S. M.; Abdel-Rahman, E. M.; El-Saadany, E. F.& Mansour, R. R. (2008). A wideband vibration-based energy harvester. *J. Micromech. Microeng.*, Vol 18, 115021.

Sun, C.; Qin, L.; Li, F.; Wang, Q.-M. (2009). Piezoelectric Energy Harvesting using Single Crystal $Pb(Mg_{1/3}Nb_{2/3})O_3 - xPbTiO_3$ (PMN-PT) Device. *J. Intell. Mat. Syst. Struct.*, Vol. 20(5), 559-568.

Taylor, G. W.; Burns, J. R.; Kammann, S. M.; Powers, W. B. & Welsh, T. R. (2001). The Energy Harvesting Eel: A Small Subsurface Ocean/River Power Generator. *IEEE J. Oceanic Eng.*, Vol. 26, 539-547.

Vullers, R.J.M.; van Schaijk, R.; Doms, I.; Van Hoof, C. & R. Mertens (2009). Micropower energy harvesting. *Solid-State Electronics*, Vol. 53, 684-693.

Zhu, D.; Tudor, M. J. & Beeby, S. P. (2010). Strategies for increasing the operating frequency range of vibration energy harvesters: a review. *Meas. Sci. Technol.*, Vol. 21, 022001.

Zhu, H.; Pruvost, S.; Guyomar, D. & Khodayari, A. (2009). Thermal energy harvesting from $Pb\left(Zn_{1/3}Nb_{2/3}\right)_{0.955}Ti_{0.045}O_3$ single crystals phase transitions. *J. Appl. Phys.*, Vol. 106, 124102.

Part 2

Memories

6

Future Memory Technology and Ferroelectric Memory as an Ultimate Memory Solution

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1. Introduction

Silicon industries have notched up notable achievements of computer-related technology over the past two decades, leading to rapid progression in information technology (IT). As a result of such a great improvement in IT applications, it is now not unusual to find mobile applications such as personal digital assistants, mobile phones with digital cameras, smart phones, smart pads able to access the Internet and hand-held personal computers. These mobile applications currently require an array of single-functioned conventional memories as they are not sufficient individually in functionality, but must combine their separate functions.

For example, dynamic random access memory (DRAM) is capable of processing massive amounts of data speedily (e.g., main memory in personal computers and servers). DRAM is highly scalable (several gigabit are commonly accessible), but requires lots of power consumption even in stand-by mode (~10^{-3} Ampere) because of the necessity of refreshing cycles in its operation. By contrast, static random access memory (SRAM) saves power[1] because its stand-by current is a few micro-Amperes. The demerit of SRAM is not readily to make it high density. This is due to the fact that its unit memory element consists of four complementary metal-oxide-semiconductor (CMOS) transistors along with two conventional transistors. SRAM's cost-benefit ratio is too high because the 6 components need much more area per unit bit memory. Data retention of both DRAM and SRAM is volatile in bit-storing nature when power goes off. In contrast to these two memories, flash memory is non-volatile. However, operation voltage during either write or erase on flash memory is too high to use the raw voltage-level of power input, *Vcc* (the term of *Vcc* comes from collector to collector voltage in a bipolar transistor). Thus during the write or erase operation, internal dummy operation (so called "charge pump") are used to pump up the input power *Vcc* to 5 times more than *Vcc* level; this is crucial in flash memory devices due to imbalance of read and write energy. The reason why the memory needs to boost the write/erase voltage up to such a high level is that hot carriers, e.g., high energy electrons, are forced to be injected through tunnel oxide to a floating gate of the transistor structure. As a result, there are two kinds of performance restrictions for use of IT applications. Writing speed of flash memory is not fast enough of an order of several milliseconds. That

[1]This is not necessarily true because the stand-by current of SRAM begins to exceed DRAM's in a deep sub micron scale due to involvement of high field junction.

makes the erasing speed of the device to be in the range of tenths of seconds. Another drawback of the device is endurance, which is defined as cycle times to write data in a memory cell. Generally, while write endurance of DRAM and SRAM is more than 10^{15} cycle[2] (10^{15} corresponds to equivalent 10 years for use), flash memory has approximately 10^{6} cycles at most as writing endurance. In addition to flash memory, there is another non-volatile memory, so called electrically erasable and programmable read only memory (EEPROM). However, EEPROM has the same limitations in flash memory due to structural and operational similarity of the unit memory cell in flash memory.

To compensate for the aforementioned disadvantages of conventional memory devices, mobile applications in the IT world have adopted a combination of individual memories, which give several penalties such as a large volume of space to pack them all and complex time adjustments to synchronize them as well. As needs of IT technology are pushing forward to many functional requirements including much faster Internet access and far more image processing, this combining approach has a limitation to apply them to those for mobile uses. Therefore, it is strongly desirable to develop an ultimate memory solution as a single memory platform, possessing positive features of the individual memories but excluding their disadvantages. The feature of the ideal memory should have fast operation for speedy communication, high density for massive data-processing, non-volatility and low power consumption for portable applications.

Among many candidates of ideal memory devices, a memory device to use ferroelectric properties, so called ferroelectric random access memory (FRAM), was proposed and experimentally explored in terms of 512-bit memory density (Evans & Womack, 1988). This is because its functional feature is similar to that of an ideal memory. This is thanks to the bi-stable state of ferroelectrics at near ambient temperature. There are several important characteristics worth mentioning. First, since core circuitry for the memory does not require stand-by power during quiescent state and the information remains unchanged even with no power supplied, it is thus *non-volatile*. Second, configuration of unit memory element is similar to that either of flash or of DRAM, allowing it to potentially become *cost-effective* high density memory. Third, *speed* of ferroelectric memory could be very close to those of the conventional volatile memories such as DRAM and SRAM. This is, in practice, because repeating the polarization reversal-read and write operation, does not need boost up base voltage unlike flash memory, stemming from balance of read and write energy of the same order of magnitude (Kryder & Kim, 2009). A good example of this is that, according to literature published recently, one of the FRAMs as a non-volatile memory has attractive memory performance such as fast access time of 1.6 GB/sec, negligible stand-by current of less than 10 micro-Ampere, and low voltage operation of less than 2.0 V even in read and write action without erase operation (Shiga et al., 2009; Jung et al., 2008). Since then, there have been tremendous improvements in FRAM developments, migrating from sub-micron to nano scale in technology node. As such, this chapter is categorized into two: First demonstrates

[2]Provided a clock frequency f of a microprocessor in an embedded system is 20 MHz (the fastest one in 2006 is about 5 MHz), reference counts necessary for cycle times per a year, is less than 1E13 in spite of considering 2% of strong data-locality in data memory. Note, the reference counts per a second is proportional to the products of frL, where f is a clock frequency, r is ratio of number of cycles in read and write operation to unit cycle and L is a constant of representing data-access locality. We will discuss this more in section 3.2.

reminiscent of how memory technologies penetrate technological barriers to match the Moore's law. Also, authors are here trying to give an insight of how silicon technology can evolve even in 20-30 nm technology node. Second is devoted to ferroelectric memories as an ultimate memory solution in many aspects such as lifetime data-retention and endurance; size effects; integration technologies; and feasibility as a fusion memory element.

2. Future memory technology

2.1 Evolution of silicon technology

2.1.1 Moore's law

It is generally accepted that semiconductor industry will continue to expand rapidly due to steady growth of the mobile, digital consumer and entertainment markets. In addition to these, many more growth engines will appear, encompassing the automotive, information-technology, biotechnology, health, robotic and aerospace industries. The advances in silicon technology that has been the backbone of tremendous previous growth, were foreseen in 1965 when Gordon Moore published his famous prediction about the constant growth rate of chip complexity (Moore, 1965). And, in fact, it has repeatedly been shown that the number of transistors integrated into silicon chips has indeed doubled every 18 months. Increases in packing density, according to the Moore's law, are driven by two factors: reductions in production costs and increases in chip performance. Another prominent example of the unstoppable pace of technology advancement[3], has been predicted (Hwang, 2006). Figure 1 shows Moore's doubling phenomena of the number of components–the number of gate in case of CPU (central processing unit) and density in memory device.

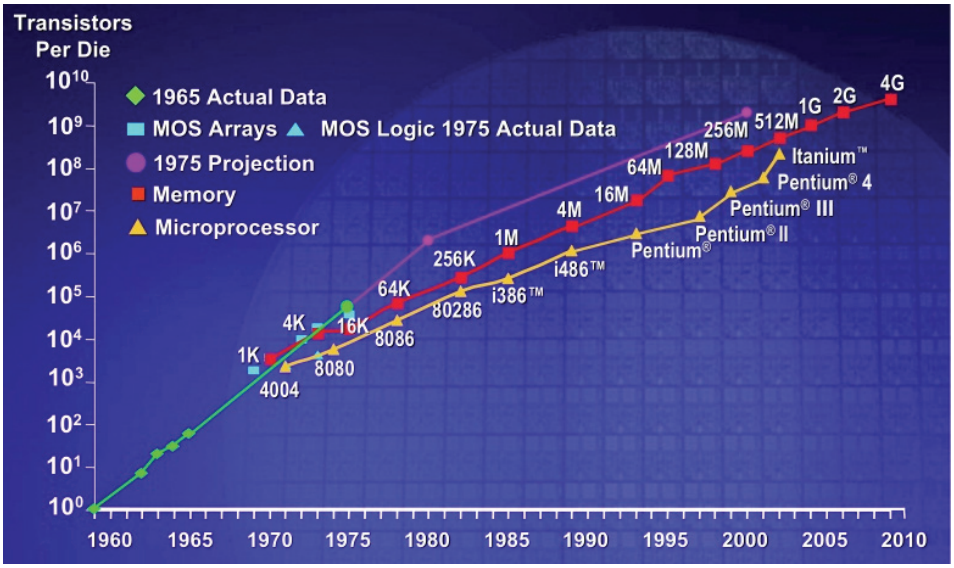

Fig. 1. Moore's doubling phenomena of the number of chips (Moore, 2006).

[3]Moore's law was predicted to stagnate to the end of the 20th century, but new sources of momentum are able to maintain or acclerate a growth trend. SoC (System-on-a-chip) integration has the potential to continue IC (integrated-circuit) cost reduction and to perpetrate growth of personal Internet products.

Despite these bright prospects, there is growing concern about whether semiconductor technology can continue to keep pace with demand when silicon technology enters the "deep nano-scale" dimension. This is because there are limits to transistor scaling, and narrowing margins in manufacturing due to ever-increasing fabrication costs tied to technical complexities (Kim & Jeong, 2005; Kim & Choi, 2006). The manufacturing cost grows because the engineering becomes more complex as transistors shrink in size. The scale is staggering, but the current generation of memory chips is 30 nm node across. This does mean that innovation is more process driven, and may require suppliers to think about what customers need and value, rather than simply pushing for ever greater density of transistors. Though most experts believe that silicon technology will maintain its leadership down to 20 nm, beyond this node a number of fundamental and application-specific obstacles will prevent further shrinkage. A common example is the inevitable occurrence of variations due to rough line edges and surfaces when pattern sizes approach atomic scales (Hwang, 2006). It is therefore the primary aim of this section to present various possible paths to overcome these obstacles and eventually to maintain the technology-scaling trend beyond 20 nm node.

As will be shown, these solutions include not only 3-D (three-dimensional) technologies but also non-silicon technologies on a molecular scale. In addition, new applications, and new growth engines for the semiconductor industry will be provided from a combination of separate technologies such as silicon-based IT with new materials (Whang et al., 2003; Wada, 2002). Therefore, this section is structured as follows: First, a review of the evolution of key silicon technologies is given. Next, we discuss scaling limits in each technology node and demonstrate practical and plausible solutions to penetrate these scaling barriers. Both DRAM and NAND flash memory are dealt with in discussion. And then, authors present prospects for the future silicon industry covering fusion technologies.

2.1.2 Evolution of silicon technology

DRAM: Since the first 1,024-bit DRAM was demonstrated by Intel™ in the early 1970's, the highest available density of DRAM has doubled every 18 months. Now DRAM technology has reached 30 nm in process technology and 4 Gb in density, which will be deployed soon in the marketplace. Further, 20-nm DRAM is being developed at R&D centers around the world. DRAM technology has evolved toward meeting a need for ever-increasing demand both of data retention and of performance improvements. Increases in data retention impose great challenges on DRAM technology by requiring not just a sufficient amount of capacitance in a memory cell but an extremely low level of leakage current from storage junction.

As device shrinks, it has been being one of the most challenging to achieve an adequate amount of cell capacitance in DRAM. It is widely agreed that the value of cell capacitance is more than 20 fF, regardless of technology-node migration. This is because sensing signal developed from memory cells, is vulnerable to become interfered by unwanted noise factors according to its operational nature. Sensing signal, Vs can be expressed by equation (1), where C_S is cell capacitance at storage node; C_{BL} is parasitic bit-line capacitance; $AIVC$ is cell array internal voltage; and the last term V_{UN} is undesirable noise. In equation (2), the first term $I_{LEAK}t_{REF}$ in the parenthesis is a term of charge loss due to junction leakage current, I_{JUNC}; gate-induced-drain-leakage (GIDL) current, I_{GIDL}; and non-generic leakage current, I_{NG}, arising from integration imperfections (e.g., dielectric leakage current and cell-to-cell leakage current) as indicated in equation (3).

$$V_S = \frac{AIVC}{2} \cdot \frac{C_S}{C_{BL} + C_S} - V_{UN} \tag{1}$$

$$V_{UN} = \frac{1}{C_{BL} + C_S}(I_{LEAK} t_{REF} + C_{BL} V_N + Q_I) \tag{2}$$

$$I_{LEAK} = I_{JUNC} + I_{GIDL} + I_{NG} \tag{3}$$

All of those loss factors are constituents of data-retention time, so called refresh time, t_{REF}. V_N is noise voltage due both to noise coupling and to mis-matches of threshold voltage and conductance of sense amplifiers. Another source of charge loss, Q_I in Eq. (2) has to be considered when DRAM is exposed to irradiations such as α-particle and cosmic rays. These undesirable components are very difficult to attenuate and become dominant as device dimensions are smaller. To maintain almost non-scalable requirement of cell capacitance of more than 20 fF/cell, dielectric material of cell capacitors have continuously evolved into high-κ dielectric materials and at the same time their structures have been pursued actively for novel ones (Lee et al., 2003a; Kim et al., 2004a). This is due to the fact that cell capacitor area decreases by a factor[4] of $1/k \sim 1/k^2$ as technology scales, where k denotes a scaling factor, where $k > 1$ (See Denard et al., 1974). In general, when designing device to a smaller dimension, the device is scaled by a transformation in three variables: dimension, voltage, and doping concentration. Firstly, all the linear dimensions are reduced by a unit-less scaling constant k, e.g., $t_{OX}' = t_{OX}/k$. Such reduction includes not only vertical dimensions such as thickness of gate oxide and junction depth, but also horizontal dimensions, for example, channel length L and width W. Secondly, voltage applied to the new device has to be reduced by the same factor, e.g., $V_{CC}'=V_{CC}/k$. Lastly, doping concentration, N_A is to be increased, e.g., $N_A' = k \cdot N_A$.

In practice, DRAM's capacitor has begun with a stacked 2-D (two-dimensional) structure, integrated under bit-line in process architecture[5] until the mid 1990's. Since then, DRAM has changed in structure to have an integration scheme of cell-capacitors placed over bit-line (COB) though there was an attempt to use trench-type capacitors, which are buried deeply in silicon substrate. In the 1990's, dielectric material of the cell capacitors has adopted silicon-based dielectrics, SiO_2/Si_3N_4, whose dielectric constant lies in between 3.9 and 7.0. With these relatively low-κ dielectrics, a cell capacitor has headed for expanding its area as much as possible. Thus, its structure has been transformed in substantially complex ways, from a simple stack to a hemi-spherical-silicon-grain (HSG) stack, to a HSG cylinder until the late 1990's. The advent of high-κ dielectrics since the beginning of 21st century has brought a new era of building the cell capacitors. Table 1 compares fundamental material properties of high-κ candidates with those of conventional low-κ dielectrics. These high-κ dielectrics have allowed us to form the cell capacitors into simpler one-cylinder-stack (OCS) than those in low-κ dielectrics due to relatively higher dielectric constant. Provided high-κ dielectric material utilizes, increase in cell capacitance will be achieved simply by increase in height of a cylinder. Such an increase in height gives rise to skyrocketing of aspect ratio of

[4]A scaling factor of capacitance $C = \varepsilon A/t$ is supposed to be $1/k$ in a 2-D stack structre, but since capacitor thickness t is not a contraint factor any more in a 3-D structure, capacitance can be written in $1/k^2$.

[5]So called capacitor-under-bit-line (CUB) in integration architecture.

cell capacitors when technology scales, together with dramatic decrease in footprint. In typical, an aspect ratio of cell capacitors ranges from 6 to 9 until 100 nm technology node. A higher aspect ratio has brought another obstacle in building cell capacitors robust: mechanical instability of OCS structures. As a result, many smart engineers in silicon industries has introduced a novel capacitor structure, supporter-added OCS such as mesh type cell capacitors, which can increase the cell capacitor height with desired mechanical stability (Kim et al., 2004a). Taking into account the recent advances of the cell-capacitor technology, the aspect ratio reaches 35 to 45, which is far beyond those of the world tallest skyscrapers, ranging from 8.6 to 10.0.

Materials	Dielectric constant (κ)	Band gap E_G (eV)	Crystal Structure(s)
SiO_2	3.9	8.9	Amorphous
Si_3N_4	7.0	5.1	Amorphous
Al_2O_3	9.0	8.7	Amorphous
Y_2O_3	15	5.6	Cubic
La_2O_3	30	4.3	Hexagonal, cubic
Ta_2O_5	26	4.5	Orthorhombic
TiO_2	80	3.5	Tetragonal, rutile, anatase
HfO_2	25	5.7	Monoclinic, tetragonal, cubic
ZrO_2	25	7.8	Monoclinic, tetragonal, cubic

Table 1. Comparison of material properties of high-κ dielectric candidates with those of conventional low-κ dielectrics (Wilk et al., 2001).

In the meanwhile, charging and discharging properties of cell capacitors depend strongly on performance of cell array transistors (CATs). On-current of the CAT plays a critical role in its charging behaviors while off-leakage current of the CAT is a decisive factor to determine their discharging characteristics. On the one hand, on-current (*Ion*) needs to be at least greater than several 10^{-6} Ampere to achieve reasonable read and write speed. On the other, off-leakage current (*Ioff*) has to satisfy a level of 10^{-16} Ampere to minimize charge loss just after charging up the cell capacitors to ensure adequate sensing-signal margin as indicated in Eq. (2). Despite continuation of technology migration, the ratio of *Ion/Ioff* has remained constant to 10^{10} approximately. CAT's technology has evolved to meet this requirement.

$$I_{ON} = \mu_{eff} \cdot C_{OX} \cdot \frac{W}{L_{eff}} \cdot \frac{(V_{GS} - V_{th})^2}{2}, \tag{4}$$

where μ_{eff} is effective mobility for electrons, C_{OX} is capacitance of gate oxide, W is width of transistor's active dimension, and L_{eff} is effective channel length.

At first, from the structural point of view, 2-D planar-type CAT (PCAT) has been moved to 3-D CAT. The reason why 3-D CAT has been adopted is to relieve data retention time. In 100-nm technology node, L_{eff} of the PCATs does not ensure a specific level of off-leakage current requirement (less than 10^{-15} A) due to high-field junction. The high electric field is caused by high-doping concentration near the channel region to block short-channel-effect (SCE). Under such a SCE circumstance, a transistor does not, in general, work any longer, by a way of punch-through between source and drain when its channel length becomes shorter. As denoted in Eq. (2) and (3), off-leakage currents I_{LEAK} are closely related to data retention

time. Generically this I_{LEAK} arises from sub-threshold current and gate-induced drain leakage (GIDL) current of cell array transistors along with junction leakage current from storage node. As L_{eff} is scaled down, the increased doping concentration against the SCE strengthens electric field across storage node junction. This increase in junction-leakage current results in degrading the data retention time (Kim et al., 1998). The degradation of data retention time becomes significant below 100 nm node due to rapid increase in junction electric field again (Kim & Jeong, 2005). This issue since the mid 2000's has been overcome by introducing 3-D cell transistors, where the junction electric-field can be greatly reduced due to lightly doped channel. One example of these newly developed structures is RCAT (Recess Channel Array Transistor) structure whose channel detours around a part of silicon substrate so that the elongated channel can be embodied in the array transistor (Kim et al., 2003). Also, the RCAT structure gives us another benefit, which lessens threshold voltage (*Vth*) due to lower doping concentration. Thereby, not only does DRAM's core circuitry operate at lower voltage but also CAT's on-current increases, as denoted in Eq. (4). Note that, according to the Moore's law, *Vcc* must be scaled down for power save. This trend has continued to come to 60 nm technology node. However, beyond 60 nm of technology node, on-current requirement has not been satisfied with such a RCAT approach alone. Thus, further innovations since 50 nm node have been pursued in a way of a negative word-line (NWL) scheme[6] in DRAM core circuitry. The NWL scheme compared with a conventional ground-word-line (GWL) scheme, allows us *Vth* reduction further, which means more on-current. However, another adverse effect on the CAT can occur as a result of the NWL. Since CAT's gate potential goes more negative during holding data stored at the storage junction, from which GIDL current increases as a function of gate-storage voltage, level of which is as high as that of gate potential compared with the conventional GWL. Many device engineers have given much effort to tackle this problem and finally have figured it out by technological implementation, for instance, mitigation of electric field exerted locally in the region overlapped between source/drain and gate in the RCAT. In pursuit of purpose, gate oxide needs to be different in thickness.

Provided that the oxide thickness in the overlapped region is thicker than that in the channel, unwanted GIDL current will decrease in proportion to electric field of the overlapped zone in the storage-node to gate (Lee et al., 2008; Jung et al., 2009). According to our calculation, one can extend this NWL-based RCATs down to 40 nm node with minor modifications (Jung et al., 2009). In 30 nm technology node, it becomes extremely difficult to achieve the successful *Ion/Ioff* ratio. A report has shown that a body-tied FinFET (fin field-effect-transistor) as a cell array transistor seems to be very promising due to its superb performances: excellent immunity against the SCE; high trans-conductance; and small sub-threshold leakage (Lee et al., 2004). For example, it allows us to have not only lower *Vth* but lower sub-threshold swing due to a fin-gate structure, providing more width for on-current and wrapping the gate for *Vth* and sub-threshold swing down. It is believed that the body-tied FinFET leads DRAM technology to be extendable down to 30 nm node. In off-leakage current, CAT's gate material has been being transformed to metal gate of higher work function (4.2~4.9 eV) instead of n+ poly-silicon gate. The lower *Vth* coming from higher work function provides us with lower channel doping. This leads to lower junction electric field and results in lower off-leakage

[6]Since a level of dc (direct current) bias at unselected word-lines is negative, sub-threshold leakage current of a cell transistor becomes extremely low because its channel has never chance to be on-set of inversion, leading to keeping a reasonable level of off-leakage current despite low Vth.

current. Figure 2 shows how DRAM's CAT structure has evolved during the past decade. Beyond 30 nm of technology node, a novel structure must be suggested for continuing the successful *Ion/Ioff* ratio. Among many structures, a vertical channel CAT (VCAT) is one of the good candidates (Yoon et al., 2006). This is because it can plausibly permit us to access an ideal transistor. A VCAT has a surrounding gate buried in silicon substrate (Kim, 2010). Bit-line connected to its data node runs buried under silicon substrate, too. With such a burying architecture, VCAT-base DRAM is expected to provide minimum size of lateral dimension per unit memory element as indicated in the inset of Fig. 2.

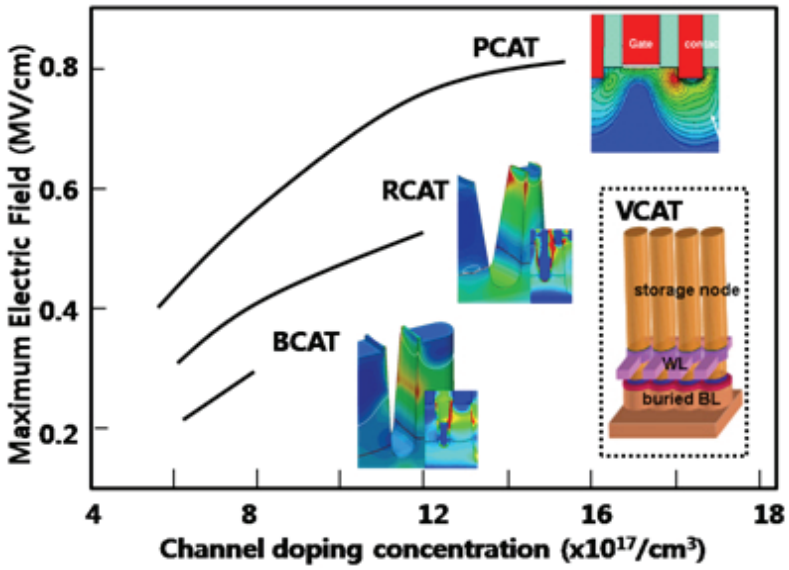

Fig. 2. Maximum electric field, E_{MAX} as a function of channel-doping concentration in various CAT's structures. As CATs evolves, the doping concentration decreases E_{MAX}, denoted in red in *E*-field strength of simulation structures as shown in the inset. An example of DRAM architecture based on VCAT is also shown in the insect.

NAND flash memory: NAND flash memory has the smallest cell size among silicon-memory devices commercially available due to its simple one transistor configuration per one bit and a serial connection of multiple cells in a string. Because of this, NAND flash has carved out a huge market for itself, as was expected since it first appeared in the mid 1980's. The need for NAND flash memory will continue to surge due to the recent resurgence of demand for mobile products such as smart phones and smart pads. With the rise of the mobile era, NAND flash has pushed toward ever-higher density, along with improving programming throughput. As a consequence, the memory has evolved toward an ever-smaller cell size in two ways: by increasing string size and by developing two bits per cell, while at the same time, increasing page depth. Now, current NAND flash memory reaches 30 nm node in process technology and 32 Gb in density, mass production of which has blossomed since the late 2000's. In addition, NAND technology beyond 30 nm is now under development at R&D centers across the world. Alongside the recent development of two-bit-per-cell technology, introduction to multi-bit cells should greatly accelerate this trend.

There are several prerequisite requirements to meet in terms of cell operation. Its cells must satisfy write and read constraints. First is programming disturbance. To program a cell, it is necessary to apply a certain amount of electric field across between floating gate and channel of the cell so that a sufficient amount of Fowler-Nordheim (FN) tunneling electrons can be injected into the floating gate.

$$\frac{1}{t_{OX}} \cdot \gamma \cdot V_{PGM} \geq \sim 10\ MeV, \qquad \gamma = \frac{C_{CS}}{C_{TUNNEL} + C_{CS}}, \tag{5}$$

where t_{OX} is thickness of tunnel oxide; γ is a coupling ratio; V_{PGM} is programming voltage; C_{CS} is capacitance between control gate and storage media; and C_{TUNNEL} is capacitance of tunnel oxide. Figure 3 illustrates (a) a schematic diagram of NAND cell arrays and (b) their programming conditions. During the programming, there are two types of unselected cells that tolerate unwanted programming: One type is cells connected to the same bit-line of the selected cell. And the other is cells connected to the same word-line. The former suffers so called V_{PASS}-stress cells while the latter endures so called V_{PGM}-stress cells as follows:

$$V_{PASS}\ stress = \frac{1}{t_{OX}} \cdot \gamma \cdot V_{PASS} \leq a\ few\ MeV, \tag{6}$$

$$V_{PGM}\ stress = \frac{1}{t_{OX}} \cdot \gamma \cdot \left[V_{PGM} - \left(1 + \frac{C_D}{\gamma \cdot C_{TUNNEL}} \right)^{-1} \right] \leq a\ few\ MeV, \tag{7}$$

where V_{PASS} stress is voltage applied to the unselected cells which share the same bit-line of the programming cell; V_{PGM} stress is voltage applied to the unselected cells which share the same word-line; and C_D is depletion capacitance of silicon substrate (See Fig. 3b). The V_{PASS}-stress and the V_{PGM}-stress are, in general, so small that neither electron injection into the unselected cells nor ejection from those is allowed in programming, respectively. Thus, V_{PASS} window is determined by allowable both V_{PASS}-stress and V_{PGM}-stress. However, the V_{PASS} window will be narrow when scaling down because of increase in depletion capacitance (C_D) as denoted in Eq. (7). Thus, as technology scales, adequate V_{PASS} window has to be satisfied. Next, in read operation, read voltage of a floating gate has to be higher than the highest threshold voltage of a cell string in order to pass read current through the string on which 32 cells are connected in series (in case of Fig. 3a). In similar to programming disturbance, read disturbance might occur in the unselected cells on the same string, and thus together with appropriate pass voltage, it is believed not only to choose tunnel oxide but to regulate its thickness in integration as well.

$$\gamma \cdot V_{READ} \geq V_{TH} \tag{8}$$

As a rule of thumb, an adequate value of the coupling ratio in read lies in the range of 0.5 ~ 0.6, and reasonable thickness of the tunnel oxide is about 80 Å. Last but not least, one of the fundamental limitations of the NAND flash stems from the number of stored charge because the available number of storage electrons decreases rapidly with technology scaling. Provided that the voltage difference between the nearest states in a 2-level cell is less than 1 V, threshold voltage shifts due to charge loss will be restricted to less than 0.5 V, which puts the limitation on charge loss tolerance as follows,

$$\Delta Q \leq C_{CS} \cdot \Delta V_{TH} = \sim 0.1Q, \tag{9}$$

In case of the floating gate, C_{CS} is C_{ONO} of capacitance of oxide-nitride-oxide. Therefore, at most 10% of charge loss is tolerable, which means that less than 10 electrons are only allowed to be lost over a 10 year period.

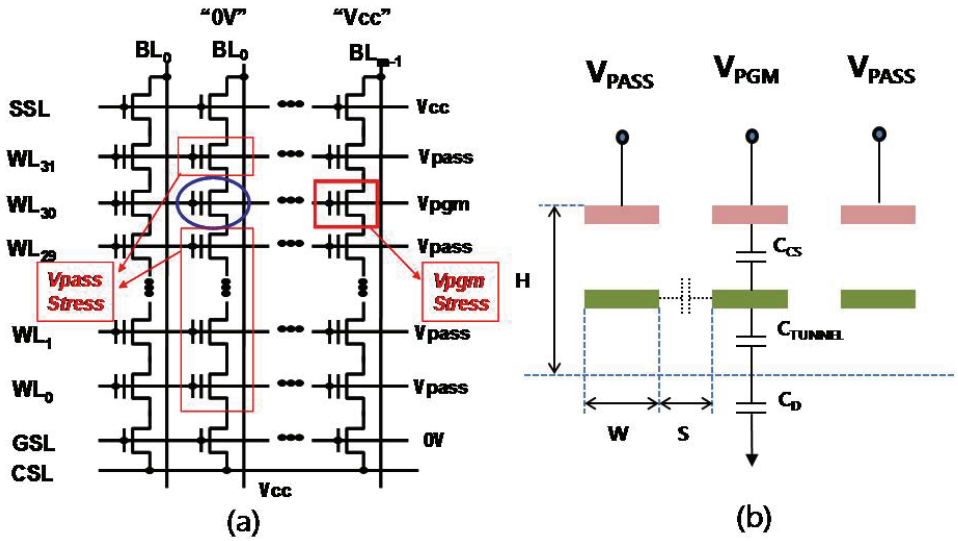

Fig. 3. (a) Schematic diagrams of memory cell arrays and (b) their programming conditions.

In technology evolution, flash memory since the late 1990's has continued to migrate technology node to 70 nm until the beginning of 2000's, based on a floating gate (FG) (Keeney, 2001; Yim et al., 2003). Due to an unprecedented growing pace of flash-memory demand for use in mobile applications, higher-grade memory in packing density has been driven by burgeoning of multi bits per a cell since the mid 2000's (Park et al., 2004; Byeon et al., 2005). Now that multi-level cell (MLC) technology means a wide range of V_{PASS} window in Eq. (5) to (7), it is essential to increase the coupling ratio as shown in Eq. (5). In addition, to overcome stringent barrier of charge-loss tolerance is simply to increase storage charge. This can also be achieved by increasing C_{CS}, as indicated in Eq. (9). However, thickness scaling for high C_{CS} may not be easy in case of C_{ONO} (e.g., a floating gate, here). This is because 60-nm flash memory has already reached 13 nm of equivalent oxide thickness (EOT[7]), which is believed to be a critical limit in thickness, for allowable charge loss–ONO thickness ~ 14.5 nm (Park et al., 2004). It has been reported that C_{CS} can be increased by replacing top-blocking oxide into new high-κ dielectric of Al_2O_3 instead. This provides us with strengthening electric field across the tunnel oxide and at the same time with lessening electric field across the blocking oxide in program and erase. Also, fast erase can be possible even at thicker tunnel oxide of over 30 Å where direct-tunneling hole current could be reduced significantly and thus such a structure gives robust data-retention characteristics (Lee et al., 2005).

Meanwhile, from the scaling point of view, flash memories have faced a serious problem since 50 nm of technology node: Cell-to-cell separation becomes so close each other that influence between adjacent cells cannot be ruled out. This is often posed not only by physical aspects of

[7]EOT indicates how thick a silicon oxide film needs to have the same effect as a different dielectric being used.

cell structures but also by certain aspects of its performance. To circumvent cell-to-cell interference, width of a floating gate tends to be more aggressively squeezed than space between floating gates (See Fig. 3b). This seems to result in a high aspect ratio of a gate stack. Such a high aspect ratio can provoke fabrication difficulty of memory cells due to its mechanical instability. And stored charge (e.g., electron) in a floating gate can redistribute easily in operational conditions, leading to vulnerability of poor data retention. Since the interference originates from another type of coupling between floating gates (FGs), it is desirable to find innovative structures, where charge storage media do not have a form of continuum of charge like the floating gate style but have a discrete sort such as charge traps (CTs) in a nitride layer. The typical examples are non-volatile memories with non-floating gate, for example, SONOS (silicon-oxide-nitride-oxide-silicon) (Mori et al., 1991), SANOS (silicon-alumina-nitride-oxide-silicon) (Lee et al., 2005), TANOS (TaN-alumina-nitride-oxide-silicon) (Shin et al., 2006) or nano-crystal dots (Tiwari et al., 1995; Nakajima et al., 1998). Recently, 32 Gb flash memory has been reported, in particular, in 40 nm of technology node (Park et al., 2006). They have pioneered a novel structure with a high-κ dielectric of Al_2O_3 as the top oxide and TaN as a top electrode. With this approach, they can achieve several essential properties for NAND flash memory: reasonable programming/erasing characteristics, an adequate V_{PASS} window for multi-bit operation and robust reliability. It is noteworthy that a TANOS structure has much better mechanical stability than that of an FG-type cell because of the far lower stack in height. Interference among TANOS cells hardly occurs due to nature of the charge trap mechanism–SiN (silicon nitride) traps act as point charges. This is the biggest advantage in CT-NAND flash memory. To scale NAND flash further down, we may need another cell technology. A FinFET could be a very promising candidate because it can increase storage electrons effectively by a way of expanding channel width of cell transistors, similar to 3-D CATs in DRAM. In this pursuit, a research group has successfully developed flash memory with a TANOS structure based on a 3-D, body-tied FinFET (Lee et al., 2006), where they can obtain excellent performance of NAND-flash cells with robust reliability. If there are much higher κ dielectrics than Al_2O_3, then we can further scale down the FinFET CT-NAND flash memory.

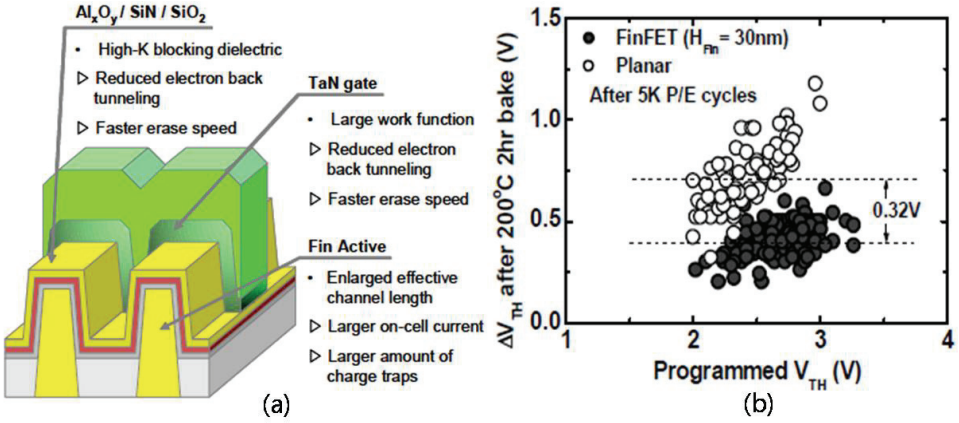

Fig. 4. (a) A schematic diagram of 3-D, body-tied FinFET NAND cells and (b) comparisons of the 3-D cells with 2-D, planar cells in threshold-voltage shift as a function of programmed threshold voltage, measured after suffering 5k program/erase cycles and a bake at 200 °C for 2 hours (Lee et al., 2006).

Figure 4 represents (a) a schematic diagram of 3-D, body-tied FinFET NAND cells and (b) comparisons of the 3-D cells with 2-D ones in threshold-voltage shift as a function of programmed threshold voltage, measured after suffering 5k program/erase cycles and a bake at 200 °C for 2 hours. The threshold-voltage delay has been improved to 0.32 V in 3-D NAND cells, compared with 2-D NAND ones.

2.2 Prospects of silicon technology

As well aware that the era of 2-D, planar-based *shrink technology* is coming to an end, semiconductor institutes have seen enormous hurdles to overcome in order to keep up with the Moore's doubling pace and thus to meet the requirements of highly demanding applications in mobile gadgetry. They have attempted to tackle those barriers by smart and versatile approaches of 3-D technology in integration hierarchy. One strand of the responses is to modify structures of elementary constituents such as DRAM's CATs, its storage capacitors and storage transistors of flash memory to 3-D ones from the 2-D. A second thread revisits these modifications to a higher level of integration: memory stacking. And another move is to upgrade this into a system in a way of fusing of each device in functionality by utilizing smart CMOS technology, e.g., *through-silicon-via* (TSV).

2.2.1 Elementary level of 3-D approach

When working with silicon devices, a transistor's key parameters must take into account: on-current; off-leakage current; the number of electrons contained in each transistor; or the number of transistors integrated. All of these factors are very important, but not equally important in functional features of silicon devices. For instance, for memory devices, off-leakage current is regarded as a more important factor and thus memory technologies tend to be developed with a greater emphasis on reducing off-leakage current. For logic, transistor delay is the single most important parameter, not just to indicate chip performance but to measure a level of excellence in device technology as well. This transistor delay is related closely to transistor's on-current state. And with 2-D planar technology in logic, one can continue to reduce transistor's channel length down to 40 nm. However, at less than 30 nm, the transistor begins to deviate in spite of a much relaxed off-current requirement. This is because of non-scalable physical parameters such as mobility, sub-threshold swing and parasitic resistance. To resolve these critical issues, two attempts have been examined. One is to enhance carrier mobility by using mobility-enhancement techniques such as strained silicon (Daembkes et al., 1986), SiGe/Ge channel (Ghani et al., 2003), or an ultra thin body of silicon (Hisamoto et al., 1989), where carrier scattering is suppressed effectively. Another approach is to reduce channel resistance by widening transistor's width. In this case, it appears very promising to use different channel structures such as tri-gate (Chau et al., 2002) or multi channel (Lee et al., 2003b). We have witnessed that, with 3-D FinFETs in memory devices, this attempt is very efficient for extending incumbent shrink technology down to 30 nm of technology node. As silicon technology scales down further, the two will eventually be merged into one single solution for an optimum level of gate control. With this type of structure, one will arrive at nearly ideal transistor performance such as being virtually free from the SCE, sufficient on-current and suppressed off-leakage current. Figure 5 shows (a) evolution trends of logic transistors in terms of EOT: A sharp decrease in EOT trend appears due to lack of gate controllability in 2-D planar structures despite high-κ dielectrics. By contrast, those in 3-D, multi-gate structures

are expected to have the same trend of EOT as those with conventional SiON dielectrics. This suggests that 3-D structures seem to become essential even with high-κ materials. It is thus believed that developing a 3-D transistor with either a multi-gate or an gate-all-around structure (Colinge et al, 1990) is quite feasible if one can extend 2-D planar technology to 3-D. This is because the channel length is no longer restricted by lateral dimension. Figure 5 also shows (b) a cross-sectional TEM (transmission-electron-micrograph) image of one of the 3-D, multi-gate transistors and (c) its *Ion-Ioff* characteristics are compared with those of 2-D planar structures.

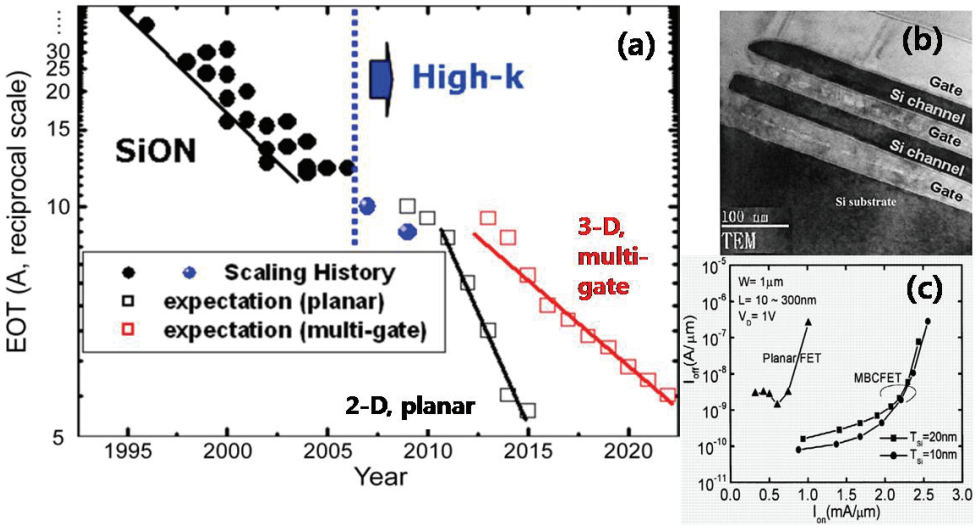

Fig. 5. (a) Equivalent-oxide-thickness (EOT) scaling trends (Kim, 2010) are shown in reciprocal scale. Due to the difficulty in controlling the SCE, a sharp decrease in EOT trend is inevitable for the coming nodes. However, the historical trend can be reverted back in the case of 3-D, multi-gate transistors. (b) A cross-sectional TEM image of a 3-D, multi-gate and (c) its *Ion-Ioff* characteristics are compared with those of the planar (Lee et al., 2003b).

2.2.2 3-D stacking of memory cells

New silicon technology based on 3-D integration has drawn much attention because it seems to be regarded as one of the practical solutions. Though the concept of 3-D integration was first proposed in the early 1980's (Kawamura et al., 1983; Akasaka & Nishimura, 1986), it has never been thoroughly investigated or verified until now, as neither silicon devices approached their limits at those times nor high-quality silicon crystal was ready for fabrication. Recent advances both in selective epitaxial silicon growth at low temperature (Neudeck et al., 2000) and in high quality layer-transferring technology with high-precision processing (Kim et al., 2004b), can bring major new momentum to the silicon industry via 3-D integration technology. The simplicity of memory architecture consisting of memory array, control logic and periphery logic, makes it relatively easy to stack one-memory cell array over another. This will ultimately lead to multiple stack designs of many different memories. Recently, one of the memory manufacturers has started to implement 3-D integration technology with SRAM to reduce large cell-size (Jung et al., 2004). Figure 6

shows (a) a cross-sectional TEM image of 3-D stacking SRAM (Left) and its schematic diagram (Right) (Jung et al., 2004): Since transistors stacked onto a given area do not need to isolate p-well to n-well, SRAM-cell size of 84 F^2 is being reduced to the extremely small cell size of 25 F^2. Encouraged by this successful approach, stacked flash memory has also been pursued. Figure 6 also represents (b) 3-D stacking NAND flash memory (Jung et al., 2006): This suggests great potential of 3-D memory stacking for large-scale use with 3-D flash-cell technology, which will spur further growth in high-density applications. Beyond 20 nm node, we believe that the most plausible way to increase density is to stack the cells vertically. Figure 6 displays (c) a 3-D schematic view of vertical NAND flash memory (Katamura et al., 2009), where SG is selecting gate, CG is control gate and PC is pipe connection. The stacking of memory cells via 3-D technology looms on the horizon, in particular, for NAND flash memory.

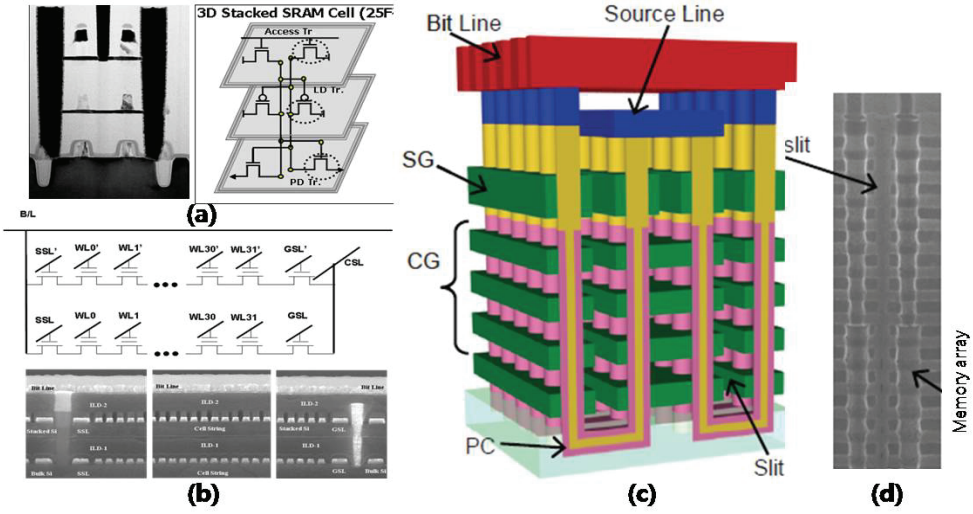

Fig. 6. (a) A cross-sectional TEM image of 3-D stacking SRAM (Left) and its schematic diagram (Right) (Jung et al., 2004). (b) 3-D stacking NAND flash memory (Jung et al., 2006). (c) A 3-D schematic view of vertical NAND flash memory (Katsumata et al., 2009), where SG is selecting gate; CG is control gate; and PC is pipe connection. (d) A cross-sectional SEM image of memory array after the removal of the sacrificial film (See Katsumata et al., 2009)

It is also believed that logic technology will shift to 3-D integration after a successful jumpstart in silicon business. The nature of a logic device, where transistors and interconnections are integrated as key elements, is not much different from those of stacked memory cells. It may be very advantageous to introduce 3-D integration technology to a logic area. Note that implementation of interconnection processes seems to be more efficient in vertical scale. For example, a dual or quad-core CPU can be realized with only a half or quarter of the chip size, which will result in significantly greater cost-effectiveness. Another promising use would be to improve logic performance by cutting down on the length of metallization. Decrease in interconnection length means a huge amount of reduction in parasitic *RC* components, i.e., a high speed and power saving. In addition, 3-D technology will make it easy to combine a memory device and a logic device onto one single chip

through hierarchical stacking. Since most parts of SoCs (system-on-chips) in the future will be allocated to memory, this combining trend will be accelerated. The next step will be to stack multi-functional electronics such as RF (radio frequency) modules, CISs (CMOS image sensors) and bio-sensors over the logic and memory layers.

2.2.3 Chip level of 3-D integration

The early version of 3-D integration in chip level has been commercialized already in a multi-chip package (MCP), where each functional chip (not device) is stacked over one another and each chip is connected by wire bonding or through the '*through-via hole*' bonding method within a single package. Figure 7 exhibits (a) a bird's eyes view of multi-chip-package (MCP) by wire bonding; (b) wafer-level stack package with through-via-hole; (c) a photograph of 3-D integrated circuit; and (d) a schematic drawing of a 3-D device for use in medical applications. The advantages of the MCP are a small footprint and better performance compared to a discrete chip solution. It is expected that the MCP approach will continue to evolve. However, the fundamental limitation of MCP will be lack of cost-effectiveness due to a number of redundancy/repair requirements. In this respect, '*through-silicon-via*' (TSV) technology is able to overcome MCP limitations through an easy implementation of redundancies and repairs. Many groups have reported TSV-based integrated circuit (TSV IC), where a single integrated circuit is built by stacking silicon wafers or dies and interconnecting them vertically so that they can function as one single device (Topol et al., 2006; Arkalgud, 2009; Chen et al., 2009). In doing so, key technologies include TSV formation, wafer-thinning capability, thin wafer handling, wafers' backside processes, and 3D-stacking processes (e.g., die-to-die, die-to-wafer and wafer-to-wafer). In detail, there are many challenging processes such as etching profiles of TSV sidewall, poor isolation liners and barrier-deposition profiles. All of these are likely to provoke TSV's reliability concerns due to lack of protection from metal (e.g., Cu) contamination. A report of silicon-based TSV interposers (Rao et al., 2009) may have advantages over traditional PCB or ceramic substrate in that it has a shorter signal routing. This results from vertical interconnect and improved reliability due to similarity to silicon-based devices in thermal expansion and extreme miniaturization in volume. TSV-IC technologies together with the 3-D interposers will accelerate an adoption of 3-D system-in-package (SiP) with heterogeneous integration (See Fig. 7d). And this might be a next momentum for genuine 3D IC devices in the future because of tremendous benefits in footprint, performance, functionality, data bandwidth, and power. Besides, as the use of 3-D silicon technology has great potential to migrate today's IT devices into a wide diversification of multi-functional gadgetry, it can also stimulate a trend that merges one technology with another, ranging from *new materials* through *new devices* to *new concepts*. In this regard, new materials may cover the followings: carbon nano-tube (CNT) (Iijima, 1991), nano-wire (NW) (Yanson et al., 1998), conducting polymer (Sirringhaus et al. 1998), and molecules (Collier et al., 1999). New devices could also be comprised of many active elements, such as tunneling transistors (Auer et al., 2001), spin transistors (Supriyo Datta & Biswajit Das, 1990), molecular transistors (Collier et al., 1999), single electron transistors (SETs) (Fulton & Dolan, 1987) and others. We may be able to extend this to new concepts, varying from nano-scale computing (DeHon, 2003) and FET decoding (Zhong et al., 2003) to lithography-free addressing (DeHon et al., 2003). To a certain extent, some of these will be readily integrated with 3-D silicon technologies. This integration will further enrich 3-D silicon technologies to create a variety of new multi-functional electronics, which will provide further substantive boosts to silicon industry, allowing us to make a projection of a nano-silicon era into practical realities tomorrow.

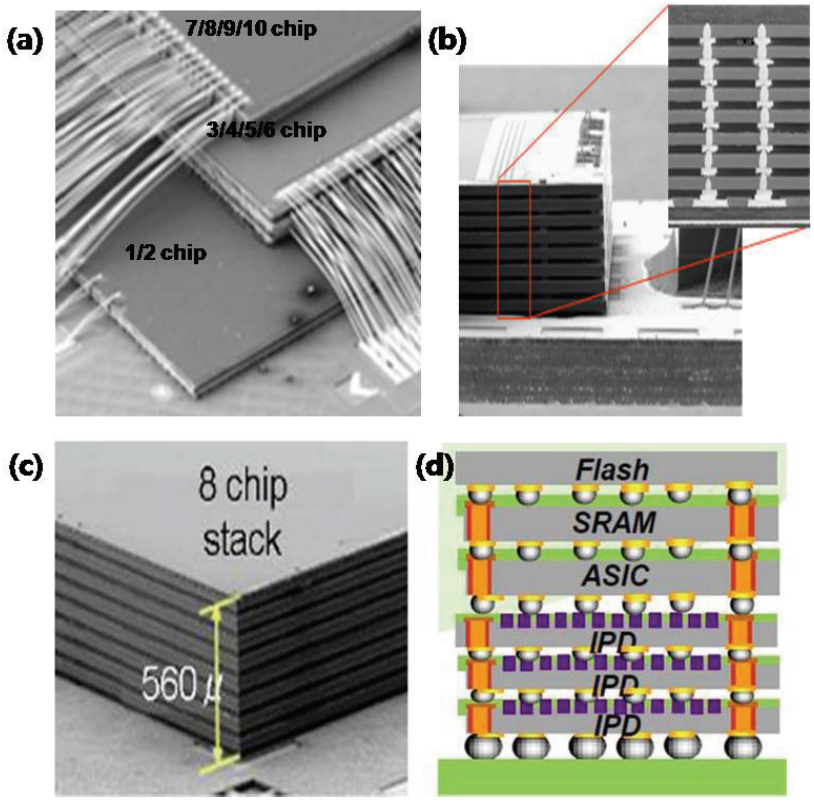

Fig. 7. (a) A bird's eyes view of (a) multi-chip-package (MCP) by wire bonding. (b) Wafer-level stack package with through-via-hole. (c) A Photograph of 3-D integrated circuit. (d) A schematic drawing of a 3-D device for medical applications enabled by TSVs and silicon interposers.

These realities will be manifested in highly desirable applications of combining of information technology (IT), bio-technology (BT), and nano-technology (NT), to become so called fusion technology (FT). Given that key obstacles to realize this are tackled by bridging the gap between previously incompatible platforms in silicon-based CMOS technology and new technological concepts, a vast number of new applications will unfold. One example may be many applications related to health sensor technology, in particular, the early recognition of cancer diseases and the screening of harmful and poisonous elements pervasive in the environment. Further, when a nano-scale bio-transistor is available, lab-on-a-chip (LoC) will become a single solution integrating all of its essential components, such as micro-array, fluidics, sensors, scanners and displayers. Then, by its very nature[8], one will have tons of benefits from a mass of disposable LoCs, which will stimulate the future silicon industry.

[8]As a successful booster for the silicon industry, whatever will be, it should be a high volume product at a reasonable price. PCs are high volume products, and hand-held phones are too. In that sense, LoC is very promising because its potential market is the entire population.

2.3 Remarks

Not only do many challenges await silicon industries as technology enters the deep nano-dimension era but promising opportunities are also there. Equipped with new technologies such as 3-D scaling and a wealth of new materials, alongside fusing of related technologies, we will overcome many hurdles ahead and respond technological challenges we will stumble along the way. All plausible solutions described earlier tell us that planar-based technology will reach an impassable limit. 3-D technology begins to provide clear signs of serving as a foundation for a refuel of the silicon industry. The advantages of 3-D integration are numerous. They include: elimination of uncertainty in the electrical characteristics of deep nano-scale transistors; extendable use of silicon infrastructures, especially optical lithography tools; and formation of a baseline for multi-functional electronics and thus facilitation of implementing a hierarchical architecture, where each layer is dedicated to a specific functional purpose. Over the next decade, we will see great endeavors in numerous areas that will greatly stimulate the semiconductor business. Successful evolutions of device structures will continue and even accelerate at a greater pace in the not-too-distant future. In addition, device designs will converge onto a single mobile platform, covering many different capacities and services from telecommunication through broadcasting and a much higher degree of data processing. In line with this, silicon technology will still play a critical role in realizing functionally merged solutions. All of these will permit us to have invaluable clues not just on how to prepare future silicon technology but also on how to positively influence the entire silicon industry. This will allow us to attain an even more sophisticated fusing of technologies. As seen in the past, silicon technology will continue to provide our society with versatile solutions and as-yet unforeseen benefits in much more cost-effective ways.

3. Ferroelectric memory as an ultimate memory solution

3.1 Introduction

There has been great interest to understand ferroelectric properties from the point of view of both fundamental physics and the need of nano-scale engineering for memory devices. On the one hand, since electric hysteresis in Rochelle salt was in 1920 discovered by Valasek (Valasek, 1921), there have been tremendous efforts to look through ferroelectricity in a comprehensive way over the past many decades. As a consequence, the phenomenological theory of ferroelectricity has been presented by many researchers: Devonshire (Devonshire, 1949; Devonshire, 1951); Jona and Shirane (Jona and Shirane, 1962); Fatuzzo and Merz (Fatuzzo and Merz, 1959); Line and Glass (Line and Glass, 1979); and Haun (Haun, 1988). The series of their works have been successful to express the internal energy of a ferroelectric crystal system. This theory has also been examined experimentally in detail, and extended by Merz (Merz, 1953); by Drougard et. al. (Drougard et al., 1955); and by Triebwasser (Triebwasser, 1956). Especially, Devonshire's phenomenological theory (Devonshire, 1949; Devonshire, 1951) gives the free energy of $BaTiO_3$ as a function of polarization and temperature. From this free energy we know what the possible state and meta-stable states of polarization are in the absence of an applied field. We also know how polarization changes as a function of field applied to the crystal. In short, according to the theory, a ferroelectric possesses two minima (e.g., a second-order phase transition) in the internal energy. These two minima are separated by an energy barrier ΔE. Essential feature of a ferroelectric is that these two minima corresponds to two different spontaneous

polarizations that can be changeable reversibly by an applied field. Under an assumption that applied electric field is able to surmount the energy barrier, the advent of smart thin-film technology in evolution of CMOS technology, has enabled to consider a ferroelectric crystal a useful application. Thinning a ferroelectric film with high purity means that there could be an opportunity to use ferroelectrics as a memory element.

On the other, integrated ferroelectrics are a subject of considerable research efforts because of their potential applications as an ultimate memory device due to 3 reasons: First, the capability of ferroelectric materials to sustain an electrical polarization in the absence of an applied field, means that integrated ferroelectric capacitors are *non-volatile*. They can retain information over a long period of time without a power supply. Second, the similar architectural configuration of memory cell-array to conventional ones, means that they are highly capable of processing *massive* amounts of data. Finally, nano-second speed of domain switching implies that they are applicable to a *high-speed* memory device. Since ferroelectric capacitors was explored for use in memory applications by Kinney et al. (Kinney et al., 1987); Evans and Womack (Evans & Womack, 1988); and Eaton et al. (Eaton et al., 1988), it has been attempted to epitomize ferroelectrics to applicable memory solutions in many aspects. In the beginning of 1990's, silicon institutes have begun to exploit ferroelectrics as an application for high-density DRAMs (Moazzami et al., 1992; Ohno et al., 1994). This is because permittivity of ferroelectrics is so high as to achieve DRAM's capacitance extremely high and thus appropriate for high density DRAMs. An early version of non-volatile ferroelectric RAM (random-access-memory) used to be several kilo bits in packing density. This lower density (NB. at that moment, DRAM had several ten mega bits in density) is because of two: One is that its memory unit was relatively large in size, being comprised of two transistors and two capacitors (2T2C) to maximize sensing signal. The other is that a ferroelectric capacitor stack has required not only novel metal electrodes such as platinum, iridium and rhodium, all of which are hard to be fine-patterned due to processing hardness, but also reluctant metal-oxide materials to conventional CMOS integration due to possible cross contaminants such as lead zircornate titanate ($PbZrTiO_3$) and strontium bismuth titanate ($Sr_{1-x}Bi_xTiO_3$). Next steps for high density non-volatile memory have been forwarded (Tanabe et al., 1995; Sumi et al., 1995; Song et al., 1999). In similar to DRAM, an attempt to build smaller unit cell in size was in the late 1990's that one transistor and one capacitor (1T1C) per unit memory was developed (Jung et al., 1998). Since then, many efforts to build high density FRAM have been pursued, leading to several ten mega bits in density during the 2000s (Lee et al., 1999; Kim et al., 2002; Kang et al., 2006; Hong et al., 2007; Jung et. al, 2008).

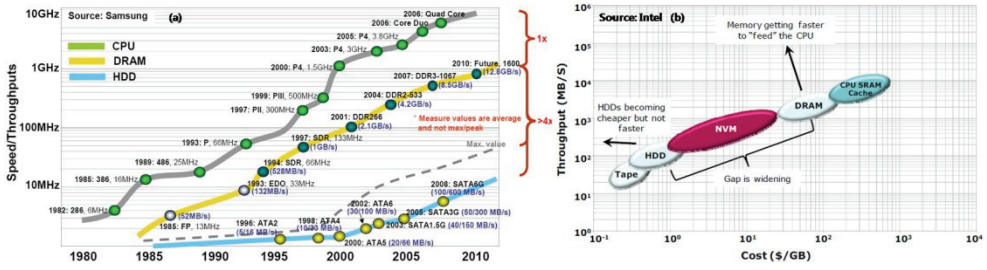

Fig. 8. (a) Evolution of electronic components in data throughput performance. (b) NVM (non-volatile memory) filling price/performance gap.

Among integrated ferroelectrics, one of the most important parameters in FRAM is sensing signal margin. The sensing signal of FRAM is proportional to remanent polarization (P_r) of a ferroelectric capacitor as follows:

$$\Delta V_{BL} = \frac{2P_r A}{C_{BL}} = \frac{2\epsilon_0 \epsilon A}{C_{BL} d}, \tag{10}$$

where A is capacitor's area; d is capacitor's thickness. As seen in equation (10), in principle, we have to compensate the area reduction when technology scales down. However, in practice, when the thickness of PZT ferroelectric thin film decreases, degradation of polarization tends to appear in the ferroelectric capacitor due to a *dead layer* between the ferroelectric and electrodes (See section 3.3.3). Unlike the requirement of DRAM's CAT, the array transistor of FRAM is not necessarily constrained from the off-leakage current due to no need of the refresh cycles, but from on-current, which is at least greater than several μA in order for a reasonable read and write speed. Thus, this will greatly relieve technology scaling quandaries and enable fast technology migration to the high end. This is because designing of a less leaky cell transistor becomes very difficult in incumbent memories such as DRAM and NAND/NOR flash due to need of lower doping concentration.

As witnessed in the Moore's law, there has been enormous improvement in VLSI (very large-scale integration) technology to implement system performance of computing platforms in many ways over the past decades. For instance, data throughput of central processing unit (CPU) has been increased by thousand times faster than that of Intel 286™ emerged in the beginning of 1980's. Alongside, a latest version of DRAM reaches a clock speed of more than 1 GHz. By contrast, state-of-the-art HDD (hard disk drive) transfers data at 600 MB/sec around (See Fig. 8a). Note that data rate of the latest HDD is still orders of magnitude slower than the processor/system-memory clock speed (see Fig. 8b). To achieve the throughput performance in more effective way, it is therefore needed to bridge performance gap in between each component. To compensate the gap between CPU and system memory, a CPU cache[9] has been required and adopted. In line with this, ferroelectric memory is non-volatile, high-speed. But it has a *destructive* read-out scheme in core circuitry, whose memory cells need to return the original state after being read. This is because the original information is destroyed after read. As a result, it is essential to return the information back to its original state, which is so-called *restore*, necessarily following the read. This operation is so inevitable in the destructive read-out memory such as DRAM and FRAM. In particular, when the ferroelectric memory are used as one of the storage devices in computing system, such as a byte-addressable non-volatile (NV)-cache device, the memory has to ensure lifetime endurance, which is regarded as the number of read/write (or erase if such operation is required) cycles that memory can withstand before loss of any of entire bit information. Thus, authors are here trying to attempt not only how FRAM provides NV-cache solutions in a multimedia storage system such as solid state disk (SSD) with performance benefits but also what should be satisfied in terms of lifetime data-retention and endurance in such applications. Here, we also put forward size effect of ferroelectric film in terms of temperature-dependent dielectric anomaly because a dead layer plays an adverse role in thickness scaling. In addition, it is very important to ensure that integration technology of FRAM in nano-dimension is extendable to one of the

[9]File system cache is an area of physical memory that stores recently used data as long as possible to permit access to the data without having read from the disk.

conventional memories. Accordingly, we will present key integration technologies for ferroelectric memory to become highly mass-productive, highly reliable and highly scalable. This covers etching technology to provide a fine-patterned cell with less damage from plasma treatments; stack technology to build a robust ferroelectric cell capacitor; encapsulation technology to protect the ferroelectric cell capacitors from process integration afterwards; and vertical conjunction technology onto ferroelectric cell capacitors for multi-level metallization processes.

3.2 Non-volatile RAM as an ultimate memory solution

SSD, one of the multimedia storage systems, in general, consists of 4 important devices. First is a micro-controller having a few hundreds of clock speed in MHz, with real-time operating system (firmware). Second is solid-state storage device such as HDD or NAND flash memory, which has several hundreds of memory size in gigabyte. Third is host interface that has the primary function of transferring data between the motherboard and the mass storage device. In particular, SATA (serial advanced technology attachment) 6G (6th generation) offers sustainable 100 MB/s of data disk rate in HDD. In addition, bandwidth required in DRAM is dominated by the serial I/O (input/output) ports whose maximum speed can reach 600 MB/s. SATA adapters can communicate over a high-speed serial cable. Last is a buffer memory playing a considerable role in system performance. As such, DRAM utilization in SSD brings us many advantages as a buffer memory. For example, in DRAM-employed SSD, not only does I/O shaping in DRAM allow us to align write-data unit fitted into NAND flash page/block size but collective write could also be possible. As a result of sequential write, the former brings a performance benefit improved by 60% at maximum, and also the latter gives us another performance benefit improved by 17% due to increase in cache function, as shown in Fig. 9a and b, respectively.

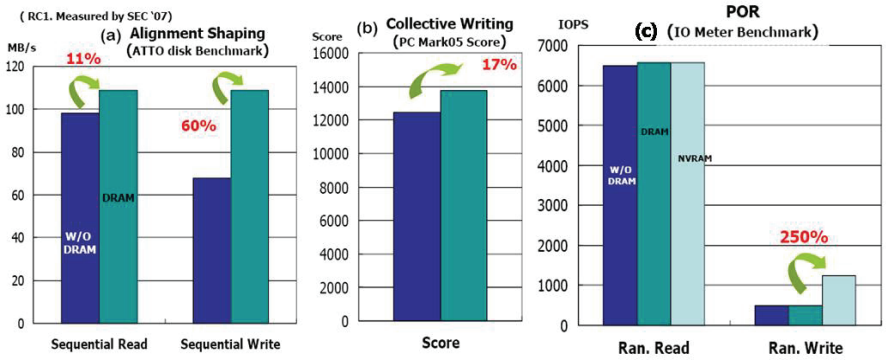

Fig. 9. Impact of DRAM utilization in SSD on system performance. (a) Increase in sequential read/write by I/O shaping. (b) Performance improvement by collective WRITE. (c) Additional performance benefit for DRAM plus FRAM in SSD.

As an attempt to implement system performance further, not only does DRAM have been considered but FRAM has also been taken into account because of its non-volatility and random accessibility. Before that, it is noteworthy that, in SSD with no NV-cache, system-log manager is needed to record and maintain log of each transaction[10] in order to ensure that

[10]Each set of operations for performing a specific task.

file system maintains consistency even during a power-failure. A log file that contains all the changes in metadata, generally serves as a history list of transactions performed by the file system over a certain period of time. Once the changes are recorded to this log, the actual operation is now executed. This is so-called power-off recovery (POR). By contrast, POR is redundant in FRAM-employed-SSD as a NV-cache because metadata can be protected by FRAM. Elimination of POR overhead is the single most critical implementation by utilization of FRAM. This is because FRAM provides such system with byte-addressable and non-volatile RAM function. Thus, in spite of sudden power failure, system can safely be protected by adopting FRAM even without POR overhead, ensuring integrity of metadata stored in the ferroelectric memory. Through many benchmark tools, we have confirmed that by eliminating this overhead, system performance has been increased by 250% in random write (See Fig. 9c). This also brings the system to no need of flush operation in file system. As a consequence, additional 9.4% increase in performance, maximizing cache-hitting ratio. Since metadata frequently updated do not necessarily go to NAND flash medium, endurance of the flash memories can be increased by 8% at maximum as well. Besides, failure rate of operations can be reduced by 20% due to firmware robustness increased mostly by elimination of the POR overhead.

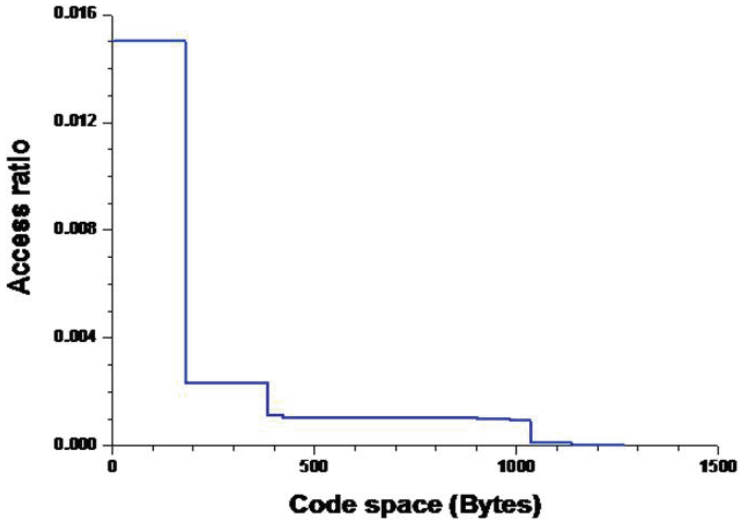

Fig. 10. Data locality of FRAM as a code memory.

Meanwhile, how many endurance cycles are necessary for use in applications of NV-cache solutions such as data memory and code memory? To answer this question, we need to understand access patterns of NV-cache devices in multimedia system. Now, we take into account the followings: First is the ratio of read/write per cycle in data memory (likewise, number of data fetching per cycle in code memory). Generally, the ratio for data memory and code memory is 1.00 and 0.75, respectively. Second is data locality[11]. Figure 10 is a simulation result showing strong locality of 1.5% when FRAM has been considered a code

[11]The locality of reference is the phenomenon that the collection of data locations often consists of relatively well predictable clusters of code space in bytes.

memory. As shown in Fig. 10, less than 200 bytes of code space is more frequently accessed. Provided wear-leveling in read/write against the strong locality and taking an example of 20 MHz clock frequency of main memory (CPU clock ~ 200 MHz), what has been found is that the endurance cycles for 10-year lifetime becomes less than 9.5×10^{13}. This number of cycles is far less than the cycles we presumably assumed, which is more than 10^{15} cycles. Thus, authors believe that more than 1.0×10^{14} of the endurance cycles is big enough to ensure that the ferroelectric memory as a NV-cache is so endurance-free as to be adopted to a multimedia storage system.

3.3 Reliabilities

3.3.1 Retention

Since Merz's exploration of domain switching kinetics in the mid 1950's (Merz, 1954), it is now believed that polarization reversal occurs in a way of domain nucleation and growth (Landauer, 1957; Pulavari & Kluebler, 1958; Key & Dunn, 1962; Du & Chen, 1997; Jung et al., 2002; Kim et al., 2005; Jo et al., 2006). The retention time of FRAM is closely related to a decay rate of the polarization reversal of a ferroelectric capacitor as expressed in formula (11).

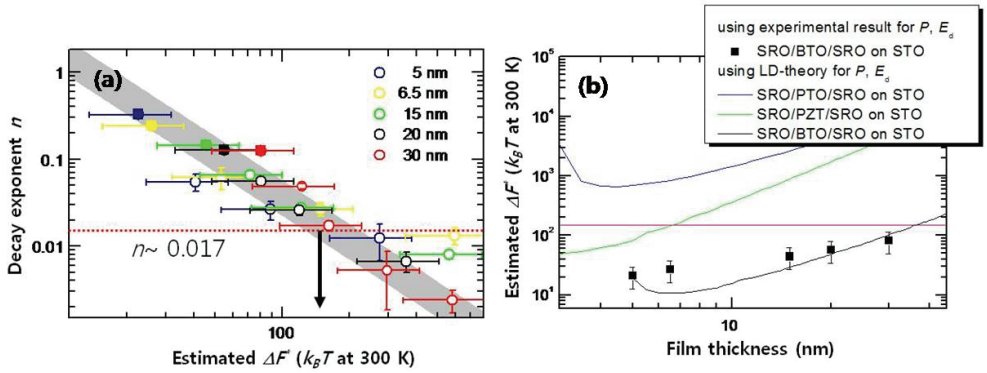

Fig. 11. (a) A decay exponent n plot against estimated thermal energy $\Delta F^*/k_BT$ in various thickness of of $BaTiO_3$ films and (b) thermal energy barrier $\Delta F^*/k_BT$ as a function of thickness in different ferroelectric stacks.

$$\frac{P(t)}{P_0} = \left(\frac{t}{t_0}\right)^{-n} \tag{11}$$

$$\Delta F^* = -2EP_SV + \sigma_w A + U_d \tag{12}$$

where P_0 is initial remanent polarization; $P(t)$ is remanent polarization at time t; t_0 is a time constant; n is an exponent; ΔF^* is domain free energy; E is homogeneous electric field applied externally; V is the volume of domain nucleus; σ_w is domain wall energy; A is domain wall area. While the first term of Eq. (12) represents the electrostatic energy gained by formation of a domain nucleus, the second is the surface energy, and the last term is the field energy of the depolarizing field (Merz, 1954). Provided that length of domain nuclei is much smaller than thickness of a ferroelectric, half-prolate spheroidal nuclei tends to be formed and finally reaches a cylindrical shape (Key & Dunn, 1962; Jung et al., 2002). Under such an assumption, if one can measure depolarization energy of Eq. (12), we can now

estimate $\Delta F^*/k_BT$, where k_B is Boltzmann constant. Based on experimental values of depolarization field E_d that ranges from 300 to 800 kV/cm (Kim et al., 2005), the corresponding $\Delta F^*/k_BT$ is estimated to 4 to 20 at ambient temperature (Jo et al., 2006). Figure 11 represents (a) a decay exponent n plot against estimated thermal energy $\Delta F^*/k_BT$ in various thickness of $BaTiO_3$ films and (b) thermal energy barrier $\Delta F^*/k_BT$ as a function of thickness in different ferroelectric stacks. As seen in Fig. 11a, in most of interesting nano-ferroelectrics with thickness ranging from 5 to 30 nm, the energy barrier is evaluated to $\Delta F^*/k_BT \sim 150\ k_BT$ for $n \sim 0.017$, which is the exponent corresponding to 50% of polarization decay during 10 years in Eq. (11). Thus, as shown in Fig. 11b, if one takes into account a stack of $SrRuO_3$-$PbTiO_3$-$SrRuO_3$ (SRO-PTO-SRO), the energy barrier of polarization reversal via the formation of domain nuclei during 10 years is more than 150 k_BT, which means that there is virtually no retention conumdrum in FRAM as long as a ferroelectric stack is properly chosen.

3.3.2 Endurance

In FRAM, it is not readily achieved to assure whether or not a memory device can endure virtually infinite read/write cycles. This is because of memory size that is several tens or hundreds megabits typically. For instance, a HTOL (high temperature operational life) test during 2 weeks at 125 °C, is merely a few millions of endurance cycles for each memory cell in 64-Mb memory size, for example. Even taking into account minimum number of cells (in this case 128 bits because of 16 I/Os), time to take evaluation of 10^{13} cycles is at least more than 20 days. Therefore, it is essential to find acceleration factors to estimate device endurance through measurable quantities such as voltage and temperature. However, direct extraction of acceleration factors from memory chips is not as easy in practice as it seems to be in theory. This is because VLSI circuit consists of many discrete CMOS components that have a temperature and voltage range to work. Generally, more than 125 °C is supposed to be a limit to operate properly. A voltage range of a memory device is also specified in given technology node (±10% of V_{DD}=1.8 V in this case). Despite those difficulties, it has been attempted to figure out acceleration factors in terms of temperature and voltage, together with information obtained from capacitor-level tests.

In regard to package-level endurance, figure 12 represents changes in (a) peak-to-peak sensing margin (*SMpp*) and (b) tail-to-tail sensing margin (*SMtt*) as read/write cycles continues to stress devices cumulatively at 125 °C. Both *SMpp* and *SMtt* have been obtained by averaging out 30 package samples for each stress voltage. Function-failed packages have been observed when *SMpp* and *SMtt* reach 10% and 25% loss of each initial value, respectively. As seen in Fig. 12a and b, voltage acceleration factors (AF_V) between 2.0 V and 2.5 V has been calculated by these criteria (AF_V = 81 at *SMpp* and AF_V = 665 at *SMtt*). In other words, the test FRAMs can endure 1×10^{12} of read/write cycles at the condition of 125 °C and 2.0 V. Second, in capacitor-level endurance, figure 13 is (a) a normalized polarization plot against cumulative fatigue cycles at 145 °C in a variable voltage range and (b) a logarithm plot of cycle-to-failure (CTF) as a function of stress voltage in a various range of temperature. Here, we introduce a term of CTF which is referred to as an endurance cycle at which remanent polarization (or sensing margin) has a reasonable value for cell capacitors (or memory) to operate. Polarization drops gradually as fatigue cycles increase and the collapsing rate is accelerated as stress voltage goes higher. Likewise, provided 10% loss of polarization is criteria of CTF, the CTF at 145 °C and 2.0 V approximates 2.2×10^{12}. (NB. This

is reasonable because samples of 10% loss in *SMpp* turned out to be defective functionally.) Considering temperature- and voltage-acceleration factors from Fig. 13a, acceleration condition of 145 °C, 3.5V is more stressful in 5 orders of magnitude than that of 85 °C, 2.0 V. In other words, 1.0×10^9 of CTF at 145 °C, 3.5 V is equivalent to 6.0×10^{14} at 85 °C, 2.0 V.

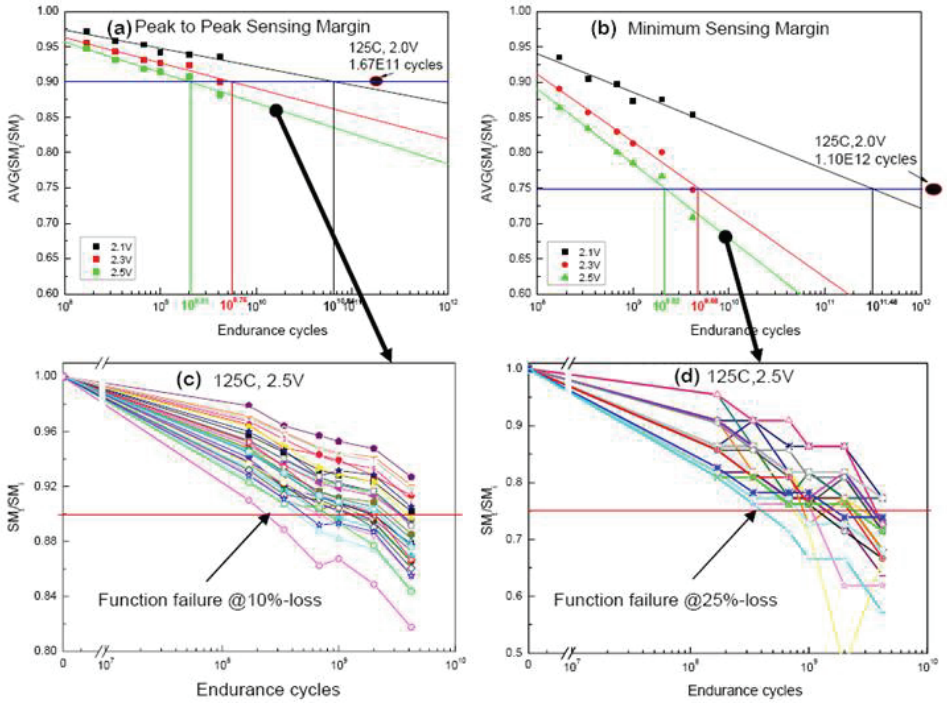

Fig. 12. Changes in (a) peak-to-peak sensing margin (*SMpp*) and (b) tail-to-tail sensing margin (*SMtt*) as a function of endurance cycles at 125 °C. (c) *SMpp* vs. endurance cycles at 125 °C, 2.5 V. (d) *SMtt* vs. endurance cycles at 125 °C, 2.5 V. *SMt* and *SMi* of the ordinate in Fig. 12a and b is sensing margin at time *t* and initial time, respectively.

Results of the acceleration factors obtained from device-level tests differ from those in capacitor-level. For example, while AF_V(2.5 V/2.0 V) of 81 in device-level tests[12], that of 16 in capacitor-level. We have yet to find a reasonable clue of what makes this difference. But it could be thought that the difference might arise from the fact that a memory device contains many different functional circuitries such as voltage-latch sense amplifiers, word-line/plate-line drivers, all of which make tiny amount of voltage difference magnify each effect on cell capacitors. This tendency can also be observed in the big gap of AF_V obtained from two different definitions between *SMtt* (AF_V = 665) and *SMpp* (AF_V = 81). Tail-bit behaviors of memory cells could include a certain amount of extrinsic imperfection, in general. Thus, we believe that results tested in capacitor-level seem to be close to a fundamental nature of CTF

[12]It is thought that AFV in capacitor-level tests follows AFV of SMpp in device-level rather than that of SMtt because of nature of capacitor-level tests that average out all the cell capacitor connected in parallel.

than those in device-level tests due to lack of extrinsic components. Figure 14 is (a) a logarithm plot of CTF as stress voltage increases in a various range of temperature and (b) Weibull distribution of endurance life in package samples tested at 125 °C in a various voltage range. The distributions in a 2.2-3.0 V range of voltage have a similar shape parameter, m~2.4. This suggests that evaluation of endurance tests in device-level makes sense in physical term. As seen in Fig. 14a, voltage-endurance stress at less than 2.0 V does not allow us to obtain any sign of degradation in sensing margins within a measurable time span. Nor does temperature-endurance stress above 125 °C due to off-limits of operational specifications of the device.

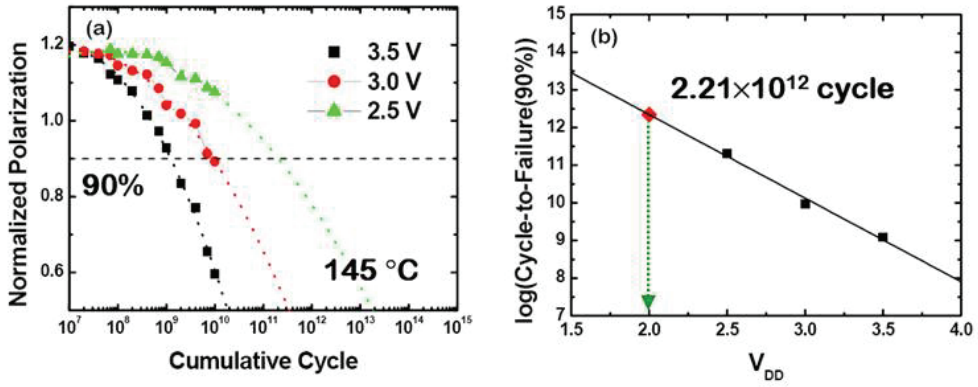

Fig. 13. (a) A normalized polarization plot against cumulative fatigue cycles at 145 °C in a variable voltage range. (b) Logarithm of CTF vs. stress voltage, V_{DD} at 145 °C.

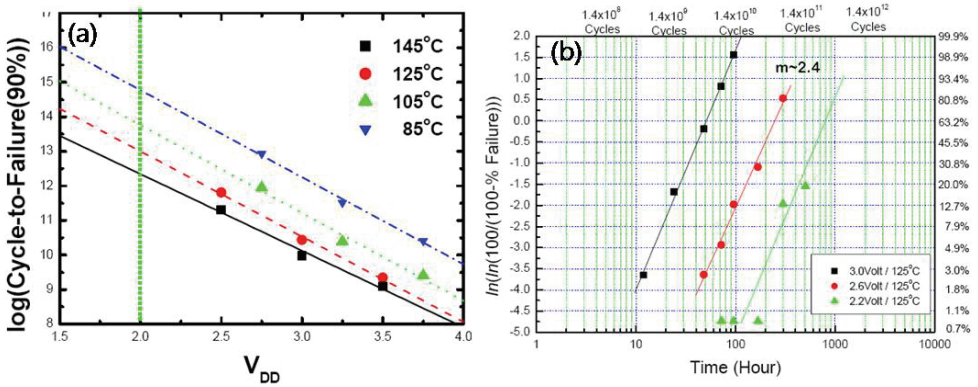

Fig. 14. (a) A logarithm plot of CTF as stress voltage increases in a various range of temperature and (b) distributions of endurance life in device-level tests at 125 °C.

3.3.3 Temperature-dependent dielectric anomaly

Since ferroelectricity involves the cooperative alignment of electric dipoles responding external field applied, there should be a critical volume below which the total energy associated with domain nucleation and growth, is outweighed by the entropic desire to

disorder. There has been a trend in recent literature to use the term "size effect" relating to the stability of spontaneous polarization to specifically describe the manner in which reduced size leads to progressive collapse of ferroelectricity (Saad et al., 2006). Finding the point at which this size-driven phase transition occurs is obviously interesting and fundamentally important, and thus various groups have done excellent works to elucidate, via both theory (Li et al., 2996; Junquera & Ghosez, 2003) and experiment (Streiffer et al., 2002; Tybell et al., 1999; Nagarajan et al., 2004), the dimensions at which ferroelectricity is lost. In that sense, one of the most critical quantities in ferroelectrics is remanent polarization P_r, which can be expressed as below:

$$P_r^2 \approx P_S^2 = -\frac{\alpha}{\beta}, \tag{13}$$

$$\text{and} \quad \frac{1}{\epsilon_0 \epsilon_r} \approx \frac{1}{\chi} = -2\alpha = -\frac{2(T - T_C)}{\epsilon_0 C}, \tag{14}$$

where P_S is spontaneous polarization; α and β are standard bulk LGD (Landau-Ginzburg-Devonshire) coefficients, provided that ferroelectric materials have a second-order phase transition while neglecting the P^6 terms due to lack of contribution in the free energy expansion of the LGD theory (then, a hysteresis loop would be a cubic equation); χ is the dielectric susceptibility; T_C is the transition temperature; and C is the *Curie* constant. As denoted in Eq. (10) and (13), the sensing signal depends strongly on spontaneous polarization P_S, which is also varying material constants such as α and β. Eq. (14) is temperature-dependent dielectric *anomaly*, so-called, the *Curie-Weiss* law. Thus, in this section, we will examine whether or not size effect of ferroelectrics is intrinsic.

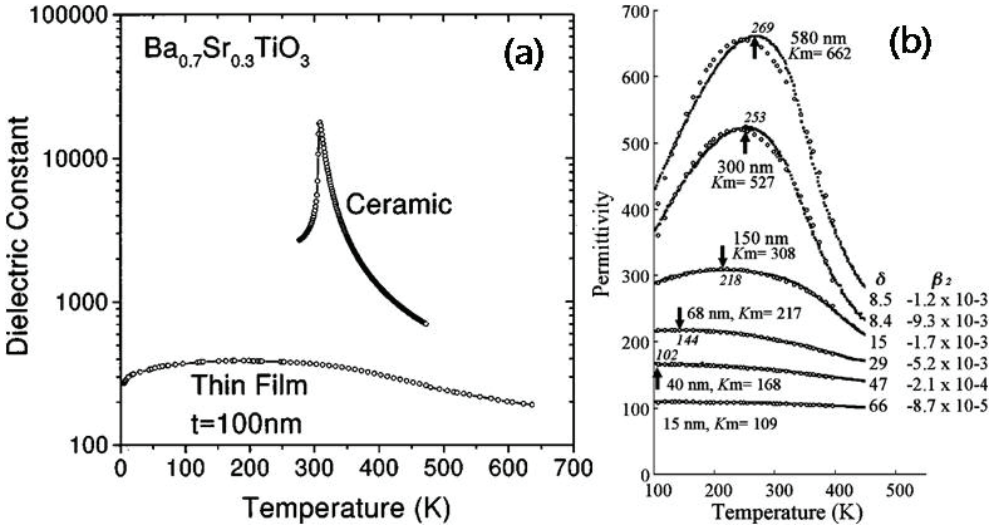

Fig. 15. Changes in dielectric constants as a function of temperature in BST materials: (a) Comparison of temperature-dependent dielectric constants between a ceramic bulk and a film 100-nm thick (Shaw et al., 1999). (b) Variation of relative permittivity as a function of temperature with a variety of thickness ranging from 15 to 580 nm (Parker et al., 2002)

In many ferroelectrics, ferroelectric phenomena could be ascribed to a dielectric origin, so-called, temperature dependent dielectric *anomaly* (Wieder, 1958; Pulavari & Kluebler, 1958). Since most integrated ferroelectrics are embedded as a thin film, it is desirable to pay much attention to the temperature-dependent dielectric properties in thin-film ferroelectrics. In this regard, there have recently been good approaches to evaluate size effects of ferroelectrics on their dielectric behaviors, in particular, in terms of temperature dependence. Figure 15 shows changes in the dielectric constant as a function of temperature in $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) materials. As seen in Fig. 15a, Shaw et al. (Shaw et al., 1999) observed that temperature-dependent dielectric constant in a $Ba_{0.7}Sr_{0.3}TiO_3$ bulk ceramic undergoes sudden change in value i.e., a first-order transition near ambient temperature at which a peak of dielectric constant in thin-film $Ba_{0.7}Sr_{0.3}TiO_3$ 100 nm thick, suffers a collapse of dielectric constant by orders of magnitude with severe broadening of *Curie* anomaly. This suggests a second-order transition. Along with the observation of Shaw et al., Parker et al. (Parker et al., 2002) measured variations of dielectric constant as a function of temperature over a variety of thickness ranging from 15 to 580 nm for $Ba_{0.7}Sr_{0.3}TiO_3$. They found that the temperature dependence of the dielectric constant exhibits diffusive shapes, also suggesting second-order transitions shown in Fig. 15b. They also found that the temperature maxima in the relative permittivity plots tend to decrease as the film thickness decreases, implying reduction of the transition temperature, T_C.

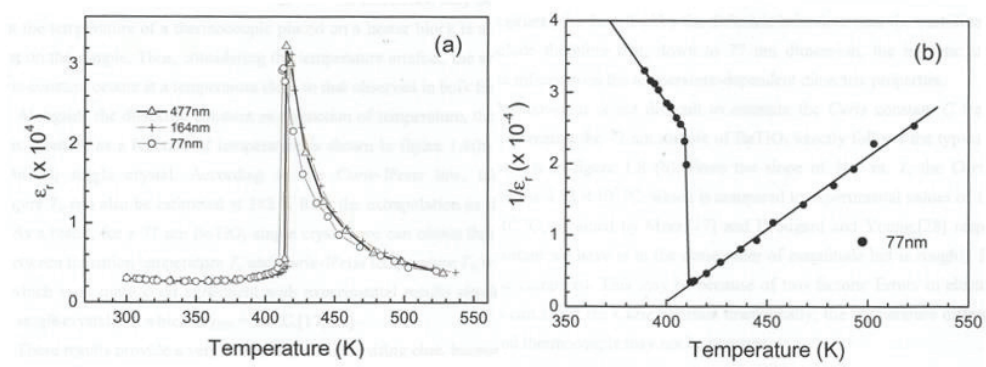

Fig. 16. (a) A relative permittivity plot as a function of temperature in $BaTiO_3$ of single crystal with a variety of thickness that ranges from 447 to 77 nm. (b) The inverse of relative permittivity plot as a function of temperature in $BaTiO_3$ crystal 77-nm thick (Saad et al., 2006).

There are many possible origins to explain these temperature-dependent dielectric properties: First, these effects could arise from an intrinsic size effect that results in a drop in permittivity with decreasing sample dimension. Second is a model suggesting that a dead layer of grain boundary in BST films could have a low permittivity value compared to that of their grain interior; although the microstructure in the films has a columnar shape, resulting in a parallel rather than series capacitance contribution. Third, this is because of structural imperfection at film-electrode interfaces, consisting of interfacial dead layers and the biaxial strain caused by the thermal expansion mismatch with the substrate (Shaw et al., 1999; Parker et al., 2002). It is necessary to know whether the first case weights less severely

than the others, because the first is instrinsic. In this respect, Saad et al. (Saad et al., 2004a, 2004b) devised a method to thin bulk single-crystal $BaTiO_3$ using a focused ion beam (FIB) in order to evaluate the size effects of single crystal ferroelectrics thus excluding grain boundaries. The dielectric behaviors as a function of temperature in $BaTiO_3$ single crystals has been evaluated with a range of thickness from 447 nm to 77 nm (Morrison et al., 2005), fabricated from a bulk single crystal $BaTiO_3$. Figure 16 shows (a) a relative permittivity plot as a function of temperature in these single crystals of $BaTiO_3$ and (b) the reciprocal relative permittivity plot of the 77 nm $BaTiO_3$ as a function of temperature. Startlingly, dielectric constants have similar behavior to that of bulk $BaTiO_3$ single crystal even down to 77 nm thick. The dielectric constant in $BaTiO_3$ 77 nm thick gradually decrease over a range from 2,738 to 2,478 at temperature corresponding to 300 to 365 K, considerably increases and abruptly soars up to 26,663 at 410 K. The dielectric constant reaches a peak of 26,910 at 413 K and hyperbolically dcreases as temperature increases further.

In general, the dielectric constant in bulk $BaTiO_3$ single crystal are regarded as 160 for ϵ_c (parallel to the polar axis) and 4100 for ϵ_a (normal to the polar axis) at ambient temperature (Landauer et al., 1956; Benedict & Duran, 1958). In addition, the sudden change in dielectric constants due to the phase transition from *FT* (ferroelectric, tetragonal) to *PC* (paraelectric, cubic), occurs either 122 ^oC upon heating or at 120 ^oC on cooling (Merz, 1953; Drougard & Young, 1954). In Fig. 16a, the transition temperature T_C is a little bit different from one of bulk $BaTiO_3$.[13] Morrison et al. (Morrison et al., 2005), however, think that this difference may be caused by the fact that the temperature of thermocouple placed on a heater block is a little bit higher than that on the sample. Thus, considering the temperature artefact, the abrupt change in dielectric constant occurs at a temperature close to that observed in bulk $BaTiO_3$. Alongside the dielectric constant as a function of temperature, the inverse of the dielectric constant as a function of temperature is shown in Fig. 16b for the 77-nm $BaTiO_3$ single crystal. According to the *Curie-Weiss* law, the *Curie-Weiss* temperature T_0 can also be estimated at 382 K from the extrapolation as shown in Fig. 16b. As a result, for the 77-nm $BaTiO_3$ single crystal, they can obtain that the difference $\Delta Temp$ between T_C and T_0 is approximately 13 ^oC, which is quite good aggreeement wth experimental results obtained from bulk $BaTiO_3$ single crystal, in which $\Delta Temp$ = 14 ^oC (Merz, 1953; Drougard & Young, 1954). These results provide a very intersesting and promising clue, because ferroelectric properties even in 77-nm thickness are expected to show a similar dielectric behavior with that of bulk $BaTiO_3$. In addition, the first-order transition from *FT* to *PC* in ferroelectrics can appropriately be decribed by the dielectric behaviors near the transition temepertures. They conclude therefore that, down to 77 nm dimension, the intrinsic size effect has negligible influence on the temperature-dependent dielectric properties. Moreover, it is not difficult to estimate the *Curie* constant *C* from the *Curie-Weiss* plot because the 77-nm sample of $BaTiO_3$ exactly follows the typical *Curie-Weiss* law as shown in Fig. 16b. From the slope of $1/\epsilon_r$ vs. *T*, the *Curie* constant is approximately 4.53×10^5 ^oC, which is compared to experimental values of 1.56×10^5 and 1.73×10^5 ^oC, obtained by Merz (Merz, 1953) and Drougard and Young (Drougard & Young, 1954), respectively. The *Curie* constant is in the same order of magnitude but is roughly 3 times larger than those compared. This may be because of two

[13]It was widely accepted that the Curie point of undoped crystal and ceramic $BaTiO_3$ was near 120 ^oC. Measurements on highly purified ceramics and on crystals grown by Remica's process (Remica & Morrison Jackson, 1954) but without the addition of Fe^{3+} have shown that their Curies temperature is near 130 ^oC (Jaffe et al., 1971).

factors: Errors in electrode area and thickness can affect the *Curie* constant dramatically; and the temperature difference between sample and thermocouple may not be constant.

3.4 Key technologies

Etching damage: It is widely accepted that as a device shrinks, node separation of cell capacitors is not readily achievable due to necessity of novel metals that served as electrodes of the MIM (Metal-Insulaor-Metal) cell capacitor, such as iridium, iridium oxide, strontium ruthenium oxide ($SrRuO_3$). In typical, remanent polarization depends heavily on processing temperature at which ferroelectric PZT ($PbZr_{0.4}Ti_{0.6}O_3$) is etched. The remanent polarization (P_r) value drops drastically as temperature of the processing chuck in an etching chamber increases. According to a report of etching impact on ferroelectrics (Jung et al., 2007), there is no direct evidence how higher-temperature etching makes a P_r value smaller. But it is believed that a certain amount of halides or halide ions might accelerate chemical reduction during the etching process at higher temperature, in particular, at the interfaces of the cell capacitors. Thus, Jung et al. (Jung et al., 2007) reported that ferroelectric cell-capacitors suffering a severe etching damage, are likely to follow bulk-limited conduction such as space-charge-limited current (SCLC), rather than those of electrode-limited.

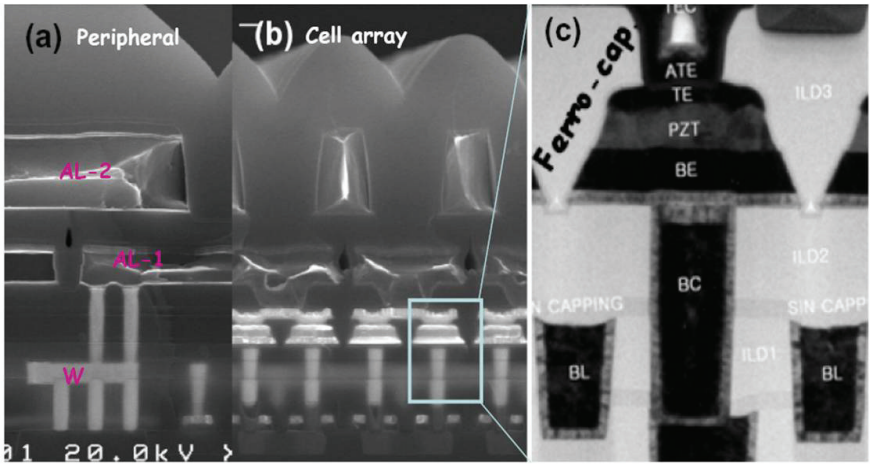

Fig. 17. Cross-sectional micrographs both (a) in a peripheral circuitry region and (b) in a cell region, (c) in which one of the cell capacitors is pictured (Jung et al., 2008).

Stack technology: Building a stack for a robust ferroelectric cell capacitor is a more important part of the entire integration than any other process due to the fact that the preparation of a ferroelectric thin-film plays a crucial role in whether the cell capacitors have the ferroelectric properties in a certain level of integration. For example, *Qos*-retention charge of a sol-gel derived PZT film is severely degraded if one evaluates non-volatile polarization by using the two-capacitor measurement technique[14]. This tells us how a ferroelectric film is

[14]Qos-retention means opposite-state charge retention that is change in non-volatile polarization values elapsed after a certain amount of time and temperature stress, before which the two capacitors are written to data 1 (D1) and data 0 (D0). In general, the Qos-retention has a faster decay rate than Qss-retention (same-state charge retention) does under the same acceleration condition because imprint change has a much more severe impact on degradation of non-volatile polarization than depolarization increases.

vulnerable to loss of ferroelectricity when film preparation is poor. The memory device integrated with CVD (chemical vapor deposition)-derived PZT film has twice bigger sensing margin than that the sol-gel-based device has even after severe suffering of a thermal acceleration test during 1000 hours at 150 ^{o}C. In addition, it is also important to regulate deposition temperature in CVD preparation of PZT films. *SMpp* of FRAM with the PZT film prepared at adequate temperature is more than 650 mV, otherwise FRAM with a less optimized PZT film has *SMpp* less than 550 mV (See Fig. 18).

Integration technologies	**Case A**	**Case B**	**Case C**	**Case D**	**Case E**	**Case F**
Etching temperature	Low	High	Low	High	High	Low
PZT deposition	Regulated	Regulated	Not	Regulated	Regulated	Regulated
Capping thickness	Thick	Thick	Thick	Thick	Thin	Thick
Recovery Anneal	No anneal	No anneal	No anneal	No anneal	No anneal	Anneal

Table 2. A list of combination of different integration conditions.

Encapsulation Technology: In general, ferroelectric capacitors comprise a perovskite-oxide-based ferroelectric film and novel metals that have a catalytic effect on oxide layers. The metallic electrodes of the ferroelectric capacitors consist of top-electrode (TE) SRO underneath iridium and bottom-electrode (BE) iridium. Due to these novel metals, oxide of the perovskite ferroelectric is very prone to chemical reduction during many hydrogen-based processes such as interlayer dielectrics (ILD) and inter-metallic dielectrics (IMD). Thus, it is essential for protecting the capacitors from these integration processes in order to build a robust capacitor. Thus, a ferroelectric cell capacitor seems to be capped with Al_2O_3 that needs to be deposited conformally on its sidewall. The Al_2O_3 layer is, typically, prepared by an atomic-layer-deposition (ALD) method. By opting a thicker Al_2O_3 layer, one can have not only a sharper distribution of bit-line potential but 33% increase in *SMpp* as well, compared with the case of an Al_2O_3 layer thinner.

Vertical conjunction: FRAM has similar architecture with one of the DRAMs, featured by folded bit-line and voltage-latch sense amplifiers. But a prominent difference between FRAM and DRAM is, in architecture, how to form the plate node of a cell capacitor–the other end is connected to the storage node of a cell transistor in both DRAM and FRAM. While a bunch of plate nodes in DRAM is connected together, a few plate nodes in FRAM should be separated. The reason of the separation is to give a plate pulse independently to each plate line. Due to this essential contact between cell capacitors and the plate lines, metallization in FRAM needs a special care in integration. This is because contact forming onto the top electrode of a cell capacitor may provoke another root-cause of capacitor degradation during the process integration. Since it is suitable for protecting ferroelectric capacitors from any involvement of aluminum when forming the plate line and strapping line, an addition-top-electrode (ATE) scheme has been adopted for this contact formation (Kim et al., 2002). The ATE landing pad consists of iridium oxide and iridium. Through a proper anneal process, what has been achieved is to decrease data 0 population of bit-line potential as low as possible, so that 8% improvement in *SMpp* is attainted.

Figure 18 summarizes (a) populations of bit-line potential as integration differently applied and (b) tail-bit populations of V_{BLD1} and V_{BLD0} for the integration scheme of the *case F* in table 2. The number of dies is 150 in total. Table 2 also summaries how each integration technology to combine. The overall population of bit-line potential has a strong impact on changes in data 1 distribution when each technology varies as shown in table 2. First,

imperfect encapsulation of the cell capacitor causes bit distribution to become wider and bigger loss of the peak value in data 1 that corresponds to switching charge quantity in ferroelectric cell capacitors. This charge lessening effect may be accelerated under the severe etching condition, for example, etching at high temperature. That is why the *case E* shows the smallest bit-line distribution in Fig. 18a in spite of the fact that the PZT thin film is properly deposited at a regulated condition. Second, when one applies a poorly regulated deposition condition to a ferroelectric thin-film preparation, broadness of cell-charge distribution appears dominantly as seen in the *case C* of Fig. 18a. Third, etching of ferroelectric capacitors in highly reduced ambient could result in tailing of data 1 distribution, giving rise to a certain loss of sensing margin as seen in the *case B* of Fig. 18a. Last, the contact formation onto the top electrode of cell capacitors should be emphasized because it might have an advantageous effect in the distribution of data 0 not only on lessening of the peak value but on being sharp without any loss of the data 1 distribution, as shown in the *case F* of Fig. 8a. Through the combination of key integration technologies, 525 mV of *SMtt* in sensing margin has been achieved (Jung et al., 2007). To recapitulate it, preparation of ferroelectric capacitors is very important to realize highly reliable and scalable FRAM. But all the integration technologies followed by the capacitor stacking is equally important, in particular, in a smaller dimension. This is because nano-scaled ferroelectric capacitors are so vulnerable as to lose the ferroelectric properties during ever-growing integration processes as reported here.

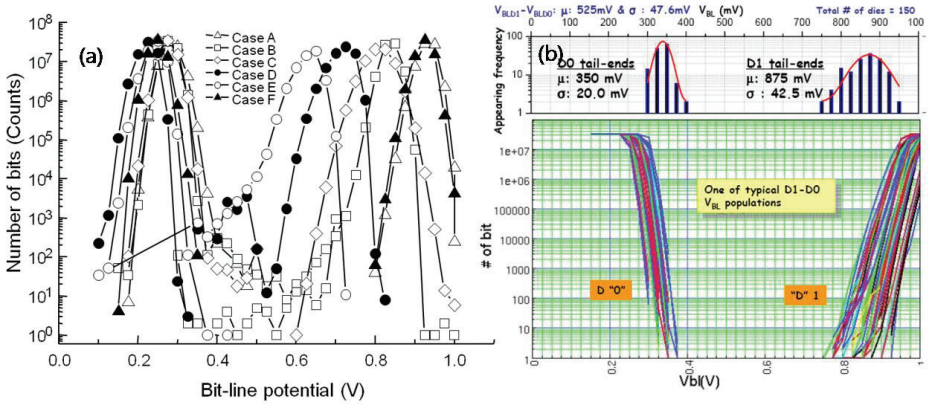

Fig. 18. (a) Data 1/Data 0 distributions of bit-line potential as integration technology varies from *case A* to *F* (See Table. 2). (b) Tail-bit populations of V_{BLD1} and V_{BLD0} for an integration scheme in table 2. The number of dies is 150 in total.

3.5 Conclusions

Utilization of FRAM as a NV-cache solution in a multimedia storage system such as SSD, gives users critical advantages. By elimination of POR overhead due to its non-volatility, random-write throughput can be enhanced by more than twice. In spite of strong data locality of FRAM, 10-year lifetime endurance has been estimated to be less than 1.0×10^{14} cycles in such system. This endurance is much less than that we presume (e.g., ~10^{15} due to every-time access for 10 years). From the investigation of acceleration factors both in device-level and in capacitor-level, CTF of the FRAM evaluated has been estimated to

approximately 6.0×10^{14} at a system operating condition. To be in a nutshell, ferroelectric memory as a NV-cache seems to be a very plausible scenario for increase in data throughput performance of SSD. In assertion of endurance, lifetime endurance is no longer problematic even in the FRAM based on a destructive read-out scheme. On top of that, the introduction of ferroelectric materials to conventional CMOS technologies has brought us to realize non-volatile, byte-addressable and high-speed memory. This is thanks not only to bi-stable states of a ferroelectric but also to tremendous efforts done by many institutes around the world, trying to epitomize it in two folds. One is, mostly done by silicon institutes, development of thin-film technology with high precision and high purity for a ferroelectric cell capacitor. The other is, mainly pursued by academia, to scrutinize thin-film ferroelectrics for whether or not their intrinsic properties (e.g., order parameters) are restricted by scaling of capacitor's thickness, so-called size effect. What both found is that ferroelectric properties is not restricted by scaling of thin ferroelectrics, at least within a concerned integration range of thickness, e.g., less than 10 unit perovskite-cells in polar axis are enough to have stable minima in dipole energy. Note that lattice constant of ferroelectrics is several Angstroms. Also, what they found is that a dead layer is not fundamental one in extremely thin ferroelectric capacitors. This suggests that gigabit density NV-RAMs by using ferroelectrics will be in the market place in the future, under an assumption that FRAM follows DRAM's approach to build ferroelectric cell capacitors in a 3-D way. Such assumption is not an illusion because physical thickness of storage dielectrics in state-of-the-art DRAM, is several ten Angstroms.

4. References

Akasaka, Y & Nishimura, T. (1986). Concept and Basic Technologies for 3D IC Structure, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 1986), pp.488-492

Arkalgud, S. (2009). Leading edge 3D technology for high volume manufacturing, *Dig. Tech. Papers, VLSI Technology Symposium*, (June 2009), pp. 68-69, 978-1-4244-3308-7

Auer, U.; Prost, W.; Agethen, M.; Tegude, F.-J.; Duschl, R. & Eberl, K. (2001). Low-voltage mobile logic module based on Si/SiGe interband tunneling devices," *IEEE Electron Dev. Lett.*, Vol. 22, (May 2001), pp.215-217, ISSN 0741-3106

Benedict, T. & Duran, J. (1958). Polarization Reversal in the Barium Titanate Hysteresis Loop, *Phys. Rev*. Vol. 109, (February 1958), pp. 1091-1093

Byeon, D.; Lee, S.; Lim, Y.; Park, J.; Han, W.; Kwak, P.; Kim, D.; Chae, D.; Moon, S.; Lee, S.; Cho, H.; Lee, J.; Kim, M.; Yang, J.; Park, Y.; Bae, D.; Choi, J.; Hur, S. & Suh, K. (2005). An 8 Gb multi-level NAND flash memory with 63 nm STI CMOS process technology, *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, (February 2005), Vol. 1, pp. 46-47, ISBN 0-7803-8904-2

Chau, R.; Doyle, B.; Kavalieros, J.; Barlage, D.; Murthy, A.; Doczy, M.; Arghavani, R. & Datta, S. (2002). Advanced Depleted-Substrate Transistors: Single-gate, Double-gate and Tri-gate, *Technical Digest, International Conference on Solid State Devices and Materials (SSDM)*, (August 2002), pp. 68-69

Chen, D.; Chiou, W.; Chen, M.; Wang, T.; Ching, K.; Tu, H.; Wu, W.; Yu, C.; Yang, K.; Chang, H.; Tseng, M.; Hsiao, C.; Lu, Y.; Hu, H.; Lin, Y.; Hsu, C.; Shue, W. & Yu, C. (2009).

Enabling 3D-IC Foundry Technologies for 28 nm Node and beyond: Through-Silicon-Via Integration with High Throughput Die-to-Wafer stacking, *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International*, (December 2009), pp.353-356, E-ISBN 978-1-4244-5640-6

Colinge, J.; Gao, M.; Romano-Rodriguez, A.; Maes, H. & Claeys, C. (1990), Silicon-on-Insulator "Gate-All-Around Device", *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International* (December 1990), pp. 595-598, ISSN 0163-1918

Collier, C.; Wong, E.; Belohradský, M.; Raymo, F.; Stoddart, J.; Kuekes, P.; Williams, R. & Heath, J. (1999). Electronically configurable molecular-based logic gates," *Science* Vol. 285, (July 1999), pp. 391–394

Daembkes, H.; Herzog, H.; Jorke, H.; Kibbel, H. & Kasper, E. (1986). The n-channel SiGe/Si modulation-doped field-effect transistor, *Electron Devices, IEEE Transactions on,* (May 1986), pp. 633-638, ISSN 0018-9383

DeHon, A. (2003). Array-based architecture for FET-based, nanoscale electronic, *IEEE Trans. Nanotechnology* Vol. 2, (March 2003), pp.23-32, ISSN 1536-125X

DeHon, A.; Lincoln, P. & Savage, J. (2003). Stochastic assembly of sublithographic nanoscale interfaces, *IEEE Trans. Nanotechnology* Vol. 2, (September 2003), pp.165-174

Denard, R.; Gaensslen, F.; Yu, H.; Rideout, V.; Bassous, E. & LeBlanc, A. (1974). Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions, *IEEE Journal of Solid-State Circuits*, Vol. SC-9, No. 5, (October 1974), pp. 256-268

Devonshire, A. (1949). Theory of barium titanate-Part I *Phil. Mag*. Vol. 40, (October 1949), pp. 1040-1063, ISSN 1941-5990 (electronic); 1941-5982 (paper)

Devonshire, A. (1951). Theory of barium titanate-Part II *Phil. Mag*. Vol. 42, (October 1951), pp. 1065-1079, ISSN 1941-5990 (electronic); 1941-5982 (paper)

Drougard, M; Landauer, R. & Young, D. (1955). Dielectric Behavior of Barium Titanate in the Paraelectric State, *Phys. Rev*. Vol. 98, (May 1955), pp. 1010-1014

Drougard, M. & Young, D. (1954). Domain Clamping Effect in Barium Titanate Single Crystals, *Phys. Rev*. Vol. 94, pp. 1561-1563 (June 1954)

Du, X. & Chen, I. (1997). Frequency Spectra of Fatigue of PZT and other Ferroelectric Thin Films. *Mat. Res. Soc. Proc.* 493, (1997), p. 311, doi 10.1557/PROC-493-311

Eaton, S.; Butler, D.; Parris, M.; Willson, D. & McNeillie, H. (1988). A ferroelectric nonvolatile memory, *Solid-State Circuits Conference, Digest of Technical Papers*, (February 1988), pp. 130–131

Evans, J. & Womack, R. (1988). An experimental 512-bit nonvolatile memory with ferroelectric storage cell, *International Electrical Electronic Engineering (IEEE) Journal of Solid-State Circuits*, Vol. 23, No. 5, (October 1988), pp. 1171-1175, ISSN 0018-9200

Fatuzzo, E & Merz, W. (1959). Switching Mechanism in Triglycine Sulfate and Other Ferroelectrics, *Phy. Rev*. Vol. 116, (October 1959), pp. 61-68

Fulton, T. & Dolan G. (1987). Observation of single-electron charging effects in small tunnel junctions, *Phys. Rev. Lett.*, Vol. 59, (July 1987), pp. 109-112, doi 10.1103/PhysRevLett.59.109

Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; McIntyre, B.; Mistry, K.; Murthy, A.; Sandford, J.; Silberstein, M.; Sivakumar, S.; Smith, P.; Zawadzki, K.; Thompson, S. & Bohr, M.

(2003). A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors, *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International,* (December 2003), pp. 11.6.1-4, ISBN 0-7803-7872-5

Haun, M. Ph.D. Thesis, (1988). *Thermodynamic theory of the lead zircornate-titanate solid solution system*, The Pennsylvania State University, 1988. Ch. 1

Hisamoto, D.; Kaga, T.; Kawamoto, Y. & Takeda, E. (1989). A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET, *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International* (December 1989), pp. 833-836 ISSN 0163-1918

Hong, Y.; Jung, D.; Kang, S.; Kim, H.; Jung, J.; Koh, H.; Park, J.; Choi, D.; Kim, S.; Ahn, W.; Kang, Y.; Kim, H.; Jung, W.; Lee, E.; Jeong, H. & Kim, K. (2007). 130 nm-technology, 0.25 um2, 1T1C FRAM Cell for SoC (System-on-a-Chip)-friendly Applications, *Tech. Papers, VLSI Technology Symposium,* (June 2007),pp. 230-231, ISBN978-4-900784-03-1

Hwang, C. (2006). New paradigms in the silicon industries, *Electron Devices Meeting, IEDMTechnical Digest. IEEE International*, (December 2006), pp. 1-8, ISBN 1-4244-0439-8

Iijima, S. (1991). Helical microtubules of graphitic carbon, *Nature*, Vol. 354, (November 1991), pp. 56-58

Jaffe, B.; Cook, W. & Jaffe, H. (1971). *Piezoelectric Ceramics*, (*Academic Press*, India, 1971), p. 70

Jo, J.; Kim, D.; Kim, Y.; Choe, S.; Song, T.; Yoon, J.; & Noh, T. (2006). Polarization Switching Dynamics Governed by the Thermodynamic Nucleation Processin Ultrathin Ferroelectric Films, *Physical Review Letters*, (December 2006), pp. 247602-1-4

Jona, F & Shirane, G. (1962). *Ferroelectric Crystals*, Pergamon Press, Oxford, Ch.1. 1962

Jung, D.; Ahn, W.; Hong, Y.; Kim, H.; Kang, Y.; Kang, J.; Lee, E.; Ko, H.; Kim, S.; Jung, W.; Kim, J.; Kang, S.; Jung, J.; Choi, D.; Lee, S. & Jeong, H. (2008). An Endurance-free Ferroelectric Random Access Memory as a Non-volatile RAM, *Tech. Papers, VLSI Technology Symposium,* (June 2008), pp. 102-103, ISBN 978-1-4244-1802-2

Jung, D.; Dawber, M.; Scott, J.; Sinammon, L. & Gregg, J. (2002). Switching dynamics in ferroelectric thin films: an experimental survey, *Integrated Ferroelectrics*, Vol. 48, 2002, pp.59-68.

Jung, D.; Lee, E.; Seo, H.; Kim, J.; Park, Y.; Oh, K. & Kim, K. (2009) Data-retention time in 40 nm of technology node, *32nd. Conference of Semiconductor in Samsung*, (December 2009)

Jung, D.; Lee, S.; Koo, B.; Hwang, Y.; Shin, D.; Lee, J.; Chun, Y.; Shin, S.; Lee, M.; Park, H.; Lee, S.; Kim, K. & Lee, J. (1998). A Highly Reliable 1T/1C Ferroelectric Memory, *Dig. Tech. Papers, VLSI Technology Symposium,* (June 1998), pp. 122-123

Jung, D.; Kim, H. & Kim, K. (2007). Key Integration Technologies for Nanoscale FRAMs, *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 54, no. 12, (December 2007), pp. 2535-2540 ISSN 0885-3010

Jung, S.; Jang, J.; Cho, W.; Cho, H.; Jeong, J.; Chang, Y.; Kim, J.; Rah, Y.; Son, Y.; Park, J.; Song, M.; Kim, K.; Lim, J.; Kim, K. (2006), Three Dimensionally Stacked NAND flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and

TANOS Structure for Beyond 30nm Node, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2006), pp. 1-4, ISBN 1-4244-0439-8

Jung, S.; Jang, J; Cho, W.; Moon, J.; Kwak, K.; Choi, B.; Hwang, B.; Lim, H.; Jeong, J.; Kim, J. & Kim, K. (2004). The Revolutionary and Truly 3-Dimensional 25F^2 SRAM Cell Technology with the smallest S^3 (Stacked Single-crystal Si) Cell, 0.16um^2, and SSTFT (Stacked Single-crystal Thin Film Transistor) for Ultra High Density SRAM, *Tech. Papers, VLSI Technology Symposium*, (June 2004), pp. 228-229, ISBN 0-7803-8289-7

Junquera, J. & Ghosez, P. (2003). Critical thickness for ferroelectricity in perovskite ultrathin films, *Nature*, vol. 422, (2003), pp. 506–509

Kang, Y.; Joo, H.; Park, J.; Kang, S.; Kim, J.; Oh, S.; Kim, H.; Kang, J.; Jung, J.; Choi, D.; Lee, E.; Lee, S.; Jeong, H. & Kim, K. (2006). World Smallest 0.34 um2 ~ COB Cell 1T1C 64Mb FRAM with New Sensing Architecture and Highly Reliable MOCVD PZT Integration Technology, *Tech. Papers, VLSI Technology Symposium*, (June 2006), pp. 124-125, ISBN 1-4244-0005-8

Katsumata, R.; Kito, M.; Fukuzumi, Y.; Kido, M.; Tanaka, H.; Komori, Y.; Ishiduki, M.; Matsunami, J.; Fujiwara, T.; Nagata, Y.; Zhang, L.; Iwata, Y.; Kirisawa, R.; Aochi, H. & Nitayama A. (2009). Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices, *Dig. Tech. Papers, VLSI Technology Symposium*, (June 2009), pp. 136 – 137, ISBN 978-1-4244-3308-7

Kawamura, S.; Sasaki, N.; Iwai, T.; Nakano, M. & Takagi, M. (1983). Three-Dimensional CMOS ICS Fabricated by Using Beam Crystallization, *Electron Device Letters, IEEE,* Vol. 4, (Octorber 1983), pp. 366-368, ISSN 0741-3106

Key, H. & Dunn, J. (1962). Thickness dependence of the nucleation field of triglycine sulphate, (December 1962). *Phil. Mag*. 7, pp. 2027-2034, ISSN 1478-6443

Keeny, S. (2001). A 130nm Generation High Density Etox Flash Memory Technology, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2001), pp. 2.5.1-4, ISBN 0-7803-7050-3

Kim, D.; Jo, J.; Kim, Y.; Chang, Y.; Lee, J.; Yoon, J.; Song, T.; &. Noh, T. (2005). Polarization Relaxation Induced by a Depolarization Field in Ultrathin Ferroelectric BaTiO3 Capacitors, *Physical Review Letters*, (December 2005), pp. 237602-1-4

Kim, D.; Kim, J.; Huh, M.; Hwang, Y.; Park, J.; Han, D.; Kim, D.; Cho, M.; Lee, B.; Hwang, H.; Song, J.; Kang, N.; Ha, G.; Song, S.; Shim, M.; Kim, S.; Kwon, J.; Park, B.; Oh, H.; Kim, H.; Woo, D.; Jeong, M.; Kim, Y.; Lee, Y.; Shin, J.; Seo, J.; Jeong, S.; Yoon, K.; Ahn, T.; Lee, J.; Hyung, Y.; Park, S.; Choi, W.; Jin, G.; Park, Y. & Kim, K. (2004a). A mechanically enhanced storage node for virtually unlimited height (MESH) capacitor aiming at sub 70nm DRAMs, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2004), pp. 69-72, ISBN: 0-7803-8684-1

Kim, H.; Song, Y.; Lee, S.; Joo, H.; Jang, N.; Jung, D.; Park, Y.; Park, S.; Lee, K.; Joo, S.; Lee, S.; Nam, S. & Kim, K. (2002). Novel integration technologies for highly manufacturable 32Mb FRAM, *Dig. Tech. Papers, VLSI Technology Symposium,* (June 2002), pp.210-211

Kim, J.; Lee, C.; Kim, S.; Chung, I.; Choi, Y.; Park, B.; Lee, J.; Kim, D.; Hwang, Y.; Hwang, D.; Hwang, H.; Park, J.; Kim, D.; Kang, N.; Cho, M.; Jeong, M.; Kim, H.; Han, J.; Kim, S.; Nam, B.; Park, H.; Chung, S.; Lee, J.; Park, J.; Kim, H.; Park, Y. & Kim, K. (2003). The breakthrough in data retention time of DRAM Using Recess-Channel-Array Transistor (RCAT) for 88nm feature size and beyond", *Dig. Tech. Papers,VLSI Technology Symposium*, (June 2003), pp. 11-12, ISBN 4-89114-033-X

Kim, K. (2010). From the future silicon technology perspective: Opportunities and challenges, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2010), pp. 1-9

Kim, K. & Choi, J. (2006). Future outlook of NAND flash technology for 40 nm node and beyond, *Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop*, (2006) pp. 9-11

Kim, K. & Jeong, G. (2005). Memory technologies in Nano-era: Challenges and Opportunities, *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, (February 2005), pp. 576-577, ISSN 0193-6530

Kim, K.; Hwang, C. & Lee, J. (1998). DRAM Technology perspective for Giga-bit era, *IEEE Transaction of Electronic Devices*, Vol.45, (March 1998), pp.598-608, ISSN 0018-9383

Kim, S.; Xue, L. & Tiwari, S. (2004b). Low Temperature Silicon Layering for Three-Dimensional Integration, *SOI Conference, 2004. Proceedings. 2004 IEEE International*, (October 2004), pp. 136-138, ISBN 0-7803-8497-0

Kinney, W.; Shepherd, W.; Miller, W.; Evans J. & Womack, R. (1987). A nonvolatile memory cell based ferroelectric storage capacitors, *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International*, (December 1987), pp. 850-853

Kryder, M. & Kim, C. (2009). After Hard Drives—What Comes Next?, *IEEE transactions on, magnetics*, Vol. 45, No. 10, (October 2009), pp. 3406-3413

Landauer, R. (1957). Electrostatic Considerations in $BaTiO_3$ Domain Formation during Polarization Reversal, *Journal of Applied Physics*, (February 1957), Vol. 28, pp. 227-234

Landauer, R; Young, D. & Drougard, M. (1956). Polarization Reversal in the Barium Titanate Hysteresis Loop, *J. Appl. Phys.* Vol. 27, (July 1956), pp. 752-758

Lee, C.; Hur, S.; Shin, Y.; Choi, J.; Park, D. & Kim, K. (2005). Charge-trapping device structure of SiO_2/SiN/high-*k* dielectric Al_2O_3 for high-density flash memory, *Appl. Phys. Lett.* Vol. 86, (April 2005), pp. 152908-1-152908-3

Lee, C.; Yoon, J.; Lee, C.; Yang, H.; Kim, K.; Kim, T.; Kang, H.; Ahn, Y.; Park, D. & Kim, K. (2004). Novel Body Tied FinFET Cell Array Transistor DRAM with Negative Word Line Operation for Sub 60nm Technology and Beyond", *Dig. Tech. Papers, VLSI Technology Symposium*, (June 2004), p.130, ISBN: 0-7803-8289-7

Lee, J.; Ahn, Y.; Park, Y.; Kim, M.; Lee, D.; Lee, K.; Cho, C.; Chung, T. & Kim, K. (2003a). Robust memory cell capacitor using multi-stack storage node for high performance in 90 nm technology and beyond, *Dig. Tech. Papers, VLSI Technology Symposium*, June 2003), pp. 57 – 58, ISBN 4-89114-033-X

Lee, J.; Lee, J.; Lee, J.; Jeong, T. & Kim, K. (2008). GiDL engineering in 50 nm of technology node, *31st. Conference of Semiconductor in Samsung*, (December 2008)

Lee, S.; Lee, J.; Choe, J.; Cho, E.; Ahn, Y.; Hwang, W.; Kim, T.; Kim, W.; Yoon, Y.; Jang, D.; Yoo, J.; Kim, D.; Park, K.; Park, D. & Ryu, B. (2006). Improved post-cycling characteristic of FinFET NAND flash, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2006), pp. 1-4, ISBN 1-4244-0438-X

Lee, S.; Jung, D.; Song, Y.; Koo, B.; Park, S.; Cho, H.; Oh, S.; Hwang, D.; Lee, S.; Lee, J.; Park, Y.; Jung, I. & Kim, K. (1999). A FRAM Technology using 1T1C Triple Metal layers for High Performance and High Density FRAMs, *Tech. Papers, VLSI Technology Symposium*, (June 1999), p. 141-142

Lee, S.; Kim, S.; Yoon, E.; Oh, C.; Chung, I.; Park, D. & Kim, K. (2003b). A novel multibridge-channel MOSFET (MBCFET): fabrication technologies and characteristics, *Nanotechnology, IEEE Transactions on* (December 2003), pp. 253-256, ISSN 1536-125X

Li, J.; Eastman, A.; Li, Z.; Foster, C.; Newnham, R. & Cross, L. (1996). Size effects in nanostructured ferroelectrics, *Phys. Lett. A*, vol. 212, pp. 341–346, 1996

Lines, M & Glass, A. (1979). *Principles and applications of ferroelectrics and related materials*, Clarendon Press, Oxford, 1979

Merz, W. (1953). Double Hysteresis Loop of $BaTiO_3$ at the Curie Point, *Phys. Rev*., Vol. 91, (August 1953), pp. 513-517

Merz, W. (1954). Domain Formation and Domain Wall Motions in Ferroelectric $BaTiO_3$ Single Crystals, *Phys. Rev.* Vol. 95, (August 1954), pp. 690–698

Moazzami, R.; Maniar, P.; Jones, R.; Campbell, A. & Mogab, C. (1992). Ultra-high charge storage capacity ferroelectric lead zirconate titanate thin films for gigabit-scale DRAMs, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 1992), pp. 973-976

Moore, G. (1965). Cramming more components onto integrated circuits, *Electronics Magazine*, 19 (April 1965). pp. 24-27

Moore, G. (2006). Moore's Law at Forty, *Understanding Moore's Law, D.C. Brock, ed., Chemical Heritage Foundation*, p. 76

Mori, S.; Sakagami, E.; Araki, H.; Kaneko, Y.; Narita, K.; Ohshima, Y.; Arai, N. & Yoshikawa, K. (1991). ONO inter-poly dielectric scaling for nonvolatile memory applications, *IEEE Transactions on Electron Devices*, Vol. 38, No. 2, (August 1991) pp. 386-391, ISSN 0018-9383

Morrison, F.; Jung, D. & Scott, J. (2005). In collaboration with Saad et al., 2004a, we independently evaluate the dielectric behaviors as a function of temperature in $BaTiO_3$ single crystal with a range from 447 to 77 nm.

Nagarajan, V; Prasertchoung, S.; Zhao, T.; Zheng, H.; Ouyang, J.; Ramesh, R.; Tian, W.; Pan, X.; Kim, D. & Eom, C. (2004). Size effects in ultrathin epitaxial ferroelectric heterostructures, *Appl. Phys. Lett.*, vol. 84, no. 25, (June 2004), pp. 5225–5227, doi:10.1063/1.1765742

Nakajima, A.; Futatsugi, T.; Nakao, H.; Usuki, T.; Horiguchi, N. & Yokoyama, N. (1998). Microstructures and electrical properties of Sn nanocrystals in thin thermally grown SiO2 formed via low energy implantation, *Journal of Applied Physics*, vol. 84, no 3, (August 1998), pp.1316-1320

Neudeck, G.; Su, T. & Denton, J. (2000). Novel Silicon Epitaxy for Advance MOSFET Devices, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2000), pp. 169-173, ISBN 0-7803-6438-4

Ohno, Y.; Horikawa, T.; Shinkawata, H.; Kashihara, K.; Kuroiwa, T.; Okudaira, T.; Hashizume, Y.; Fukumoto, K.; Eimori, T.; Shibano, T.; Arimoto, K.; Itoh, H.; Nishimura, T. & Miyoshi, H. (1994). A memory cell capacitor with BaxSr1-xTiO3 (BST) film for advanced DRAMs, *Dig. Tech. Papers, VLSI Technology Symposium*, (June 1994), pp. 149 – 150, ISBN 0-7803-1921-4

Park, J.; Hur, H.; Lee, J.; Park, J.; Sel, J.; Kim, J.; Song, S.; Lee, J.; Lee, J.; Son, S.; Kim, Y.; Park, M.; Chai, S.; Choi, J.; Chung, U.; Moon, J.; Kim, K.; Kim, K. & Byung-Il Ryu, B. (2004). 8Gb MLC (Multi-Level Cell) NAND flash Memory using 63nm Process Technology, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2004), pp. 873-876, ISBN: 0-7803-8684-1

Park, Y.; Choi, J.; Kang, C.; Lee, C.; Shin, Y.; Choi, B.; Kim, J.; Jeon, S.; Sel, J.; Park, J.; Choi, K.; Yoo, T.; Sim, J. & Kim, K. (2006). Highly manufacturable 32 Gb multi-level NAND flash memory with 0.0098 nm^2 cell size using TANOS (Si-oxide-nitride-Al_2O_3-TaN), *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2006), pp. 1-4, ISBN 1-4244-0438-X

Parker, C.; Maria, J. & Kingon, A. (2002) Temperature and thickness dependent permittivity of BaSrTiO3 thin films, *Appl. Phys. Lett*. Vol.81, (July 2002), pp. 340-342

Pulvari, C. & Kuebler, W. (1958). Polarization Reversal in Tri-Glycine Fluoberyllate and Tri-Glycine Sulfate Single Crystals, *J. Appl. Phys*. Vol. 29, (December 1958), pp. 1742-1746

Rao, V.; Ho, S.; Vincent, L.; Li, H.; Liao, E.; Nagarajan, R.; Chai, T.; Xiaowu, Z. & Damaruganath, P. (2009). TSV Interposer Fabrication for 3D IC Packaging, *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, (December 2009), p. 431, (2009), ISBN 978-1-4244-5100-5

Remeika, J. & Morrison Jackson, W. (1954). A Method for Growing Barium Titanate Single Crystals, *J. Am. Chem. Soc.*, *76* (3), (February 1954), pp. 940–941 DOI 10.1021/ja01632a107

Saad, M.; Baxter, P.; Bowman, R.; Gregg, J.; Morrison, F. & Scott, J. (2004a). Intrinsic dielectric response in ferroelectric nano-capacitors *J. Phys.: Condens. Matter* Vol. 16, (October 2004), pp. L451–L456

Saad, M.; Baxer, P.; McAneney, J.; Lookman, A.; Sinnamon, L.; Evans, P.; Schilling, A.; Adams, T.; Zhu, X.; Pollard, R.; Bowman, R.; Gregg, J.; Jung, D.; Morrison, F. & Scott, J. (2006). Investigating the effects of reduced size on the properties of ferroelectrics, *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control*, Vol. 53, (December 2006) pp.2208-2225

Saad, M.; Bowman, R. & Gregg, J. (2004b). Characteristics of single crystal thin film capacitor structures made using a focused ion beam microscope, *Appl. Phys. Lett*. Vol. 84, (February 2004), pp. 1159-1161

Shaw, T.; Suo, Z.; Huang, M.; Liniger, E.; Laibowitz, R. & Baniecki, J. (1999). The effect of stress on the dielectric properties of barium strontium titanate thin films, *Appl. Phys. Lett*. Vol. 75, (October 1999), pp. 2129-2131

Shiga, H.; Takashima, D.; Shiratake, S.; Hoya, K.; Miyakawa, T.; Ogiwara, R.; Fukuda, R.; Takizawa, R.; Hatsuda, K.; Matsuoka, F.; Nagadomi, Y.; Hashimoto, D.; Nishimura, H.; Hioka, T.; Doumae, S.; Shimizu, S.; Kawano, M.; Taguchi, T.; Watanabe, Y.; Fujii,S.; Ozaki,T.; Kanaya,H.;Kumura,Y.; Shimojo,Y.; Yamada,Y.; Minami,Y.; Sh uto, S.; Yamakawa, K.; Yamazaki, S.; Kunishima, I.; Hamamoto, T.; Nitayama, A. & Furuyama, T. (2009). A1.6 GB/s DDR2 128 Mb chain FeRAM with scalable octal bitline and sensing schemes, *Solid-State Circuits Conference, Digest of Technical Papers*, Session 27, (Feb. 2009), pp. 464–465, ISBN 978-1-4244-3458-9

Shin, Y.; Choi, J.; Kang, C.; Lee, C.; Park, K.; Lee, J.; Sel, J.; Kim, V.; Choi, B.; Sim, J.; Kim, D.; Cho, H. & Kim K. (2006) A Novel NAND-type MONOS Memory using 63nm Process Technology for Multi-Gigabit Flash EEPROMs, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 2006), pp. 327-330, ISBN 0-7803-9268-x

Sirringhaus, H.; Tessler, N. & Friend, R. (1998). Integrated Optoelectronic Devices Based on Conjugated Polymers, *Science* Vol. 280, (June 1998), pp. 1741-1744

Song, Y.; Kim, H.; Lee, S.; Jung, D.; Koo, B.; Lee, J.; Park, Y.; Cho, H.; Park, S. & Kim, K. (1999). Integration and Electrical Properties of Diffusion Barrier for High Density Ferroelectric Memory, *Applied Physics Letters*, Vol. 76, (November 1999), pp. 451-453

Streiffer, S.; Eastman, J.; Fong, D.; Thompson, C.; Munkholm, A.; Ramana Murty, M.; Auciello, O; Bai, G. & Stephenson, G. (2002). Observation of nanoscale 180 degrees stripe domains in ferroelectric PbTiO3 thin films, *Phys. Rev. Lett.*, vol. 89, (2002), no. 067601

Sumi, T.; Azuma, M.; Otsuki, T.; Gregory, J. & Araujo, C. (1995). A 0.9 V embedded ferroelectric memory for microcontrollers, *Solid-State Circuits Conference, Digest of Technical Papers*, (February 1995), pp. 70-71, ISBN 0-7803-2495-1

Supriyo Datta & Biswajit Das (1990). Electronic analog of the electro-optic modulator, *Appl. Phys. Lett.*, Vol. 56, (February 1990), pp.665-667, doi:10.1063/1.102730

Tanabe, N.; Matsuki, T.; Saitoh, S.; Takeuchi, T.; Kobayashi, S.; Nakajima, T.; Maejima, Y. ; Hayashi, Y.; Amanuma, K.; Hase, T.; Miyasaka, Y. & Kunio, T. (1995). A ferroelectric capacitor over bit-line (F-COB) cell for high density nonvolatile ferroelectric memories, *Dig. Tech. Papers, VLSI Technology Symposium*, (June 1995), pp. 123 –124, ISBN 0-7803-2602-4

Tiwari, S.; Rana, F.; Chan, K.; Hanafi, H.; Wei C. & Buchanan, D. (1995). Volatile and nonvolatile memories in silicon with nano crystal storage, *Electron Devices Meeting, IEDM Technical Digest. IEEE International*, (December 1995), pp.521-524, ISBN 0-7803-2700-4

Topol, A.; Tulipe, D.; La Shi, L.; Frank, D.; Bernstein, K.; Steen, S.; Kumar, A.; Singco, G.; Young, A.; Guarini, K.; Jeong, M. (2006). Three-dimensional integrated circuits, *IBM Journal of Research and Development,* (July 2006), pp. 491–506, ISSN 0018-8646

Triebwasser, S. (1956). Behavior of Ferroelectric $KNbO_3$ in the Vicinity of the Cubic-Tetragonal Transition, *Phys. Rev.*, Vol. 101, (February 1956), pp. 993-997

Tybell, T.; Ahn, C. & Triscone, J. (1999). Ferroelectricity in thin perovskite films, *Appl. Phys. Lett.*, vol. 75, no. 6, pp. 856–858, 1999.

Valasek, J. (1921). Piezo-electric and allied phenomena in Rochelle Salt, *Phys. Rev*. Vol. 17, (April 1921), pp. 475-481

Wada, Y. (2002). Prospects for Single-Molecule Information-Processing Devices for the Next Paradigm, *Ann. New York Acad. Sci*. 960, (April 2002), pp. 39-61

Whang, D.; Jin, S.; Wu, Y. & Lieber, C. (2003). Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems, *Nano Letters*, Vol. 3, No. 9, (July 2003), pp. 1255-1259

Wieder, H. (1958). Ferroelectric Polarization Reversal in Rochelle Salt, *Phys. Rev*. Vol. 110, (April 1958), pp. 29-36

Wilk, G.; Wallace, R. & Anthony, J. (2001). High-κ dielectrics: Current status and materials properties considerations, *Journal of Applied physics*, Vol. 89, No. 10, (January 2001), pp. 5243-5275.

Yanson, A.; Rubio Bollinger, G.; Van den Brom, H.; Agraı¨t, N. & Van Ruitenbeek, J. (1998). Formation and manipulation of a metallic wire of single gold atoms, *Nature*, Vol. 395, (October 1998), pp. 783-785

Yim, Y.; Shin, K.; Hur, S.; Lee, J.; Balk, I; Kim, H.; Chai, S.; Choi, E.; Park, M.; Eun, D.; Lee, S.; Lim, H.; Youn, S.; Lee, S.; Kim, T.; Kim, H.; Park, K & Kim, K. (2003). 70nm NAND flash technology with 0.025 μm² cell size for 4Gb flash memory, *Electron Devices Meeting*, *IEDM Technical Digest. IEEE International*, (December 1995), pp. 34.1.1-4 ISBN 0-7803-7872-5

Yoon, J.; Lee, K.; Park, S.; Kim, S.; Seo, H.; Son, Y.; Kim, B.; Chung, H.; Lee, C.; Lee, W.; Kim, D.; Park, D.; Lee, W. & Ryu, B. (2006). A Novel Low leakage Current VPT (Vertical Pillar Transistor) Integration for 4F2 DRAM Cell Array with sub 40 nm Technology, *64th Device Reearch Conference (DRC) Digest*, (June 2006), pp.259-260, ISSN 1548-3770

Zhong, Z.; Wang, D.; Cui, Y.; Bockrath, M. & Lieber, C. (2003). Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems," *Science* Vol. 302, (November 2003), pp.1377- 1379

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Ultrahigh Density Probe-based Storage Using Ferroelectric Thin Films

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1. Introduction

The probe-based seek-and-scan data storage system is an ideal candidate for future ultrahigh-density (> 1 Tbit/inch^2) nonvolatile memory devices (Vettiger et al., 2002; Pantazi et al., 2008; Hamann et al., 2006; Ahn et al., 1997; Cho et al., 2003; Cho et al., 2005; Ahn et al., 2004; Cho et al., 2006; Heck et al., 2010). In such a system, an atomic force microscope (AFM) probe (or an array of AFM probes) is used to write and read data on a nonvolatile medium; the bit size depends mainly on the radius of the probe tip. Moreover, the storage area is not defined by lithography like in SSDs, but rather by the movement of the probes. Thus improving the probe motion control to the tenth of a distance can translate into two orders of magnitude higher density. Bit size as small as 5 nm and a storage density in the Tbit/in^2 regime with data rate comparable to flash technology have been achieved (Cho et al., 2005; Cho et al., 2006). Unlike SSD technology which requires new lithographic and fabrication tools for each new generation, manufacturing of the probe-based device can be achieved using existing low-cost semiconductor equipment, which can reduce the price of these devices considerably. Another advantage of probe-based memory is that the mechanism to move the probes is low power, which reduces power consumption and heat dissipation in comparison to HDD devices.

While various writing mechanisms have been proposed for probe-based storage, e.g., thermomechanical and thermal writings on polymeric and phase-change media (Vettiger et al., 2002; Pantazi et al., 2008; Hamann et al., 2006), a great deal of attention has recently been devoted to the electrical pulse writing on ferroelectric films due to the non-structure-destructive nature of the write-erase mechanism (Ahn et al., 1997; Cho et al., 2003; Cho et al., 2005; Ahn et al., 2004; Cho et al., 2006; Heck et al., 2010). When a short electrical pulse is applied through a conductive probe on a ferroelectric film, the highly concentrated electric field can invert the polarization of a local film volume, resulting in a nonvolatile ferroelectric domain that is the basis of data recording. This mechanism allows for longer medium lifetime, i.e., larger number of write-erase cycles that is comparable to hard disk drives, faster write and read times (Forrester et al., 2009), smaller bit size (Cho et al. (2006) and higher storage densities (Cho et al. (2006).

Although the probe-based storage technology based on ferroelectric media has shown great promise, no commercial product has yet reached the market. This is mainly due to

fundamental limitations of the media material and probe-media contact during probe-sliding. For ultrahigh storage density exceeding 1 Tbit/inch^2, domain size reduction below 10 nm is required. Small domain sizes can be obtained by decreasing the size of the probe tip. However, the inverted domain is subjected to ferroelectric depolarization charges and domain-wall energy (Li et al., 2001; Wang & Woo, 2003; Kim et al., 2003) that can be high enough to invert the domain back to its initial polarization. It has been predicted (Wang & Woo, 2003) that inverted ferroelectric domains smaller than 15 nm are unstable and could be inverted back to their initial state as soon as the electric pulse is removed. This instability can be further exacerbated by the presence of a built-in electric field due to film defects present in thin ferroelectric films, which is anti-parallel to the inverted domain polarization. In short, this fundamental instability has prevented the demonstration of stable inverted domains less than 10 nm in size in ferroelectrics. Reading such sub-10 nm inverted domains at the required high speed and with high signal-to-noise ratio (SNR) is also another important issue as such a technique has to be suitable for a MEMS-based probe storage system (Heck et al., 2010).

Another technological bottleneck is that the high data access rate requires a probe-tip sliding velocity on the order of 5 to 10 mm/s, over a lifetime of 5 to 10 years, corresponding to probe-tip sliding distances of 5 to 10 km. The bit size, and thus the storage density, mainly depends on the radius of the probe-tip that is prone to rapid mechanical wear and dulling due to the high-speed contact mode operation of the system (Cho et al., 2006; Knoll et al., 2006; Bhushan et al., 2008; Gotsmann et al., 2008). This tip wear causes serious degradation of the write-read resolution over the device lifetime.

In this chapter, we review solutions that have been proposed in the literature to address the above fundamental issues and that will enable the development of probe-based nonvolatile memories with storage densities far exceeding those available in today's market. This chapter is divided into four parts. In the first part, the relevant theory and mechanism of pulse-based writing as well as probe-based storage technology on ferroelectric media are reviewed. The stability of single-digit nanometer inverted domains is addressed next. Reading schemes at high frequency and speed are then discussed. Finally a wear endurance mechanism, which allows a conductive platinum-iridium (PtIr) coated probe-tip sliding over a ferroelectric film at a 5 mm/s velocity to retain its write-read resolution over a 5 km sliding distance, is reviewed.

2. Background

Ferroelectric materials such as $BaTiO_3$ and $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) have a perovskite crystal structure in which the central atom (Ba/Zr/Ti) is bi-stable and can be shifted up or down by applying an external electric field (Figure 1a) (Ahn et al., 2004). Upon removal of the external field, the new atom polarization remains, resulting in a nonvolatile property, which is the basis of data recording. To shift the polarization of the central atom, a probe tip can be used (Figure 1b). By contacting the probe tip to the ferroelectric film and applying a bias pulse between them, a highly concentrated electric field underneath the tip is created which flips the polarization of a local volume of atoms and form an inverted polarization domain that can be used as bits for data storage (Figure 1c). The bit can be erased by applying a pulse of a reverse polarity which will switch the polarization within the written domain (Figure 1d) (Cho et al., 2003).

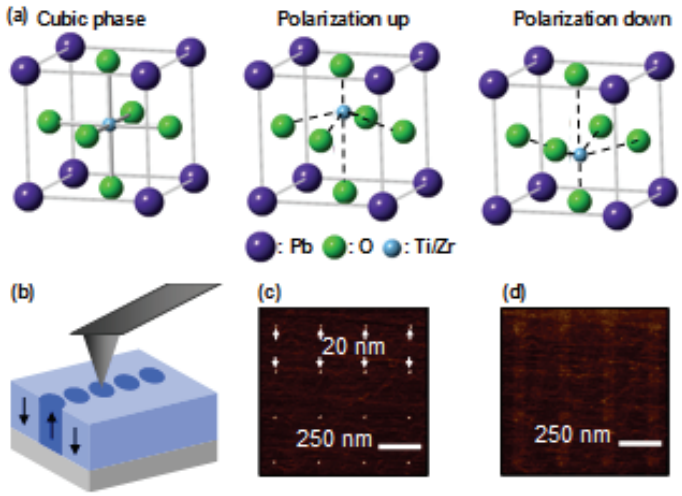

Fig. 1. Data storage on ferroelectric media. (a) Crystal structure of the perovskite ferroelectric PZT showing upward and downward polarization variants. (b) Schematic of bit writing using a probe tip to which a voltage is applied. (c) 4×4 inverted domain dot array formed on a ferroelectric medium. (d) Selective erasing of domain dots by applying a bias of reverse polarity.

The size of the volume mainly depends on the sharpness of the probe tip. In principal, the inverted volume can be as small as an individual atom, and thus allowing for a single atom memory (Ahn et al., 2004). Therefore, an ultrahigh density memory can be constructed with such a system if ultra-sharp probe tips are used and cross talk between bits is avoided. In fact, bit sizes as small as 5 nm (Figure 2a) and a storage density of 10 Tbit/in^2 with an 8 nm bit spacing have been achieved (Figure 2b) (Cho et al., 2006; Cho et al., 2005). Such a storage density is by far the highest ever achieved in any storage system. Moreover, domain switching times can be as fast as 500 ps, allowing for high writing rate (Figure 2c).

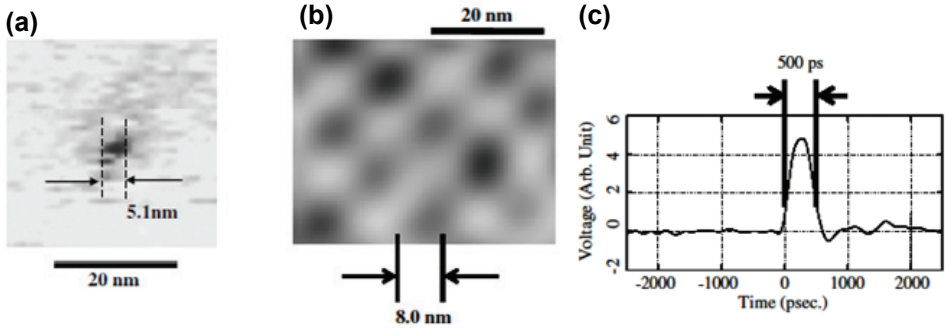

Fig. 2. Nanodomain formed using pulse writing on ferroelectric media. (a) Smallest nanodomain reported in the literature (Cho et al., 2006). (b) Highest writing density ever achieved corresponding to 10 Tbit/in2 (Cho et al., 2006). (c) 500 ps long pulse used to fully invert nanodomains in ferroelectric media (Cho et al., 2006).

Following the IBM Millipede and HP ARS systems, a joint team at Intel and Nanochip (a startup company) has recently developed a device named "seek-and-scan probe (SSP) memory device" in which the pulse writing scheme using ferroelectric media is used (Heck et al., 2010). The device architecture is shown in Figure 3 and consists of three layers. The bottom layer contains an array of 5000 MEMS cantilevers with tips that are directly fabricated on CMOS circuitry. The cantilevers are spaced at a 150 μm pitch, corresponding to the stroke of the electromagnetically actuated *x*–*y* micro-mover which forms the second layer of the device with the ferroelectric media film grown on its lower side. The third layer is a cap wafer that seals the device. The device is 15.0×13.7 mm² in size and consumes less than 750 mW with a maximum of 5% related to the MEMS actuation. It is capable of achieving a data rate of 20 Mbyte/s using 272 read-write channels. This rate is the highest ever reported in probe-based devices.

The MEMS cantilevers are fabricated directly on standard Al-backend CMOS in order to increase the overall signal-to-noise ratio (SNR) of the device. This is achieved by growing a low temperature (<455 °C) poly-SiGe film directly on the CMOS circuitry with a thin (5/10 nm) Ti/TiN interfacial layer to provide high contact resistance. This is followed by the deposition of various layers of low temperature oxide and poly-SiGe, which are micromachined to form the various parts of the free standing cantilevers. The probe-tip is defined by depositing a low-stress amorphous Si layer which is subsequently etched using various isotropic and anisotropic etching steps. Detailed fabrication steps of the device can be found in Heck et al, 2010. Figure 4 shows the MEMS cantilever design and SEM images of an individual cantilever. The probe-tips at the end of the cantilevers are brought into contact with the media by electrostatic actuators at the opposite end, which provide both vertical and lateral actuations. The vertical actuation uses a see-saw configuration with an actuation electrode. A torsional beam provides the restoring force. The lateral actuation maintains sub-nanometer positioning of the tip on the data tracks in the presence of non-uniform thermal stresses and macroscale distortion of the device.

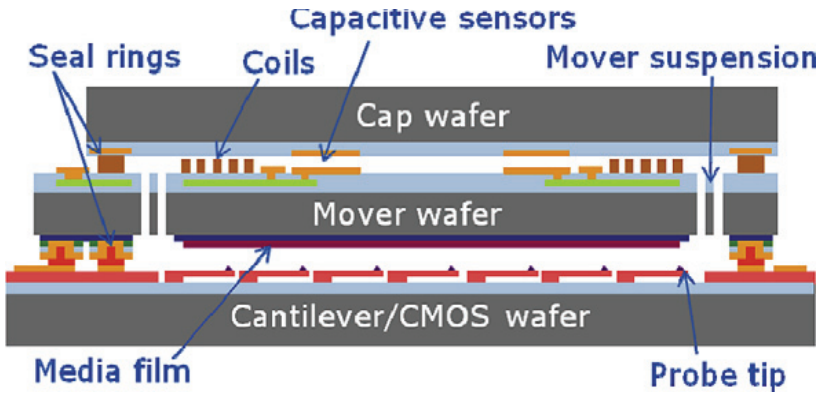

Fig. 3. Schematic of Intel SSP memory device architecture (Heck et al., 2010).

The *x*–*y* micro-mover is actuated using conductive coils on its top side in the presence of external magnets that reside in recesses in the top of the cap wafer. Micromachined suspension beams allow for high in-plane compliance while maintaining high out-of plane stiffness in order to keep a constant tip-media gap. For position sensing, capacitive sensors are fabricated on the top of the mover and the bottom of the cap. A photograph of the cap – mover assembly is shown Figure 5.

3. Stability of single-digit nanometer domains in ferroelectric films

3.1 Fully inverted ferroelectric domains

For ultra-high storage density exceeding 1 Tbit/inch^2, domain size reduction below 10 nm is required. Small domain sizes can be obtained by decreasing the size of the probe tip. Unfortunately, the inverted domain is subjected to ferroelectric depolarization charges and domain-wall energy (Li et al., 2001; Wang & Woo, 2003; Kim et al., 2003) that can be high enough to invert the domain back to its initial polarization. It has been predicted (Wang & Woo, 2003) that inverted ferroelectric domains smaller than 15 nm are unstable and could be inverted back to their initial state as soon as the electric pulse is removed. This instability can be further exacerbated by the presence of a built-in electric field due to film defects present in thin ferroelectric films, which is anti-parallel to the inverted domain polarization. In short, this fundamental instability has prevented the demonstration of stable inversion domains less than 10 nm in size in ferroelectrics.

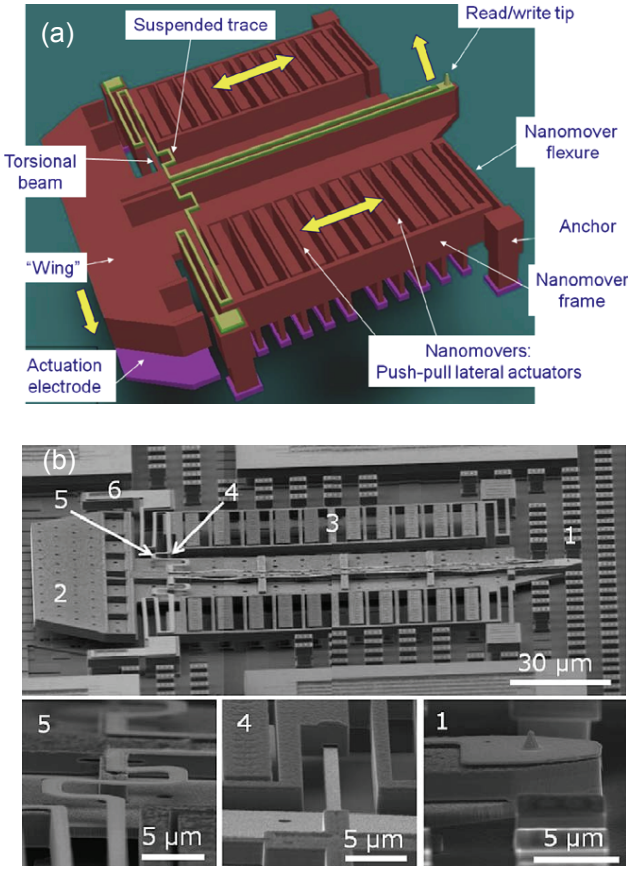

Fig. 4. Intel SSP memory device. (a) Articulated cantilever/tip design (Heck et al, 2010). (b) SEMs of an individual cantilever with probe-tip. 1: probe tip, 2: vertical actuator called wing, 3: lateral actuators called ''nanomover", 4: torsion beam for vertical actuation, 5: suspended Pt trace, 6: via between trace and CMOS (Heck et al, 2010).

Recently, our group has shown that single-digit nanometer domains remain stable if a critical ratio between probe size and ferroelectric film thickness is reached that would enable full polarization inversion through the entire ferroelectric film thickness (Tayebi et al., 2010a). To obtain reliably and repeatably sub–10 nm inverted domains, we used dielectric sheathed single-walled carbon nanotube (SWNT) prbes termed "nanopencils", which could operate in contact mode while withstanding forces as high as 14.5 μN without bending and buckling (Tayebi et al., 2008).

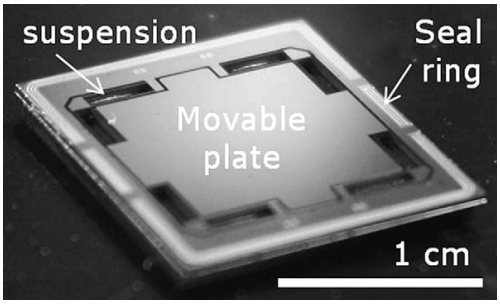

Fig. 5. Photograph of underside of cap/mover assembly (Heck et al, 2010).

Figures 6a,b show transmission electron microscopy (TEM) images of two nanopencil probes composed of a bundle of a few SWNTs (9 nm overall diameter) and of an individual SWNT (3 nm diameter), respectively. The nanopencils were used to write inverted domain dots on an atomically-smooth, single-crystalline 50-nm-thick ferroelectric PZT film grown on $SrRuO_3/SrTiO_3(100)$ substrate using metal-organic chemical vapor deposition (MOCVD) (Tayebi et al., 2008; Tayebi et al, 2010a). The film was initially polarized in an upward direction. Dot sizes as small as 11.8 nm were reliably written with the 9 nm SWNT electrode at 7 V bias pulse (Figure 6c). When trying to write the dots using the 3 nm electrode shown in Figur 6b, however, no domain inversion was recorded even at 10 Vbias pulse (Figure 6d).

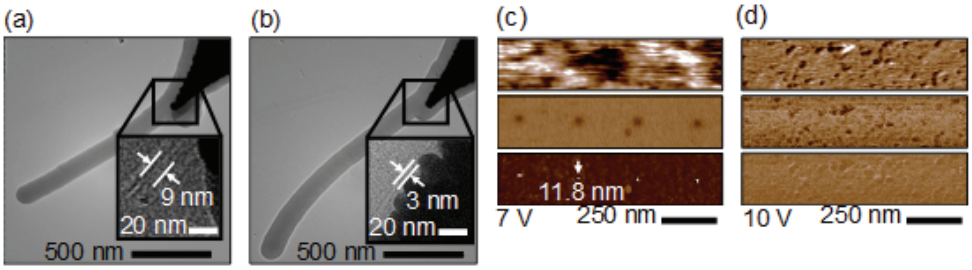

Fig. 6. SWNT-based nanopencil probe for ultra-high density probe-based storage (Tayebi et al., 2010a). (a) and (b) Transmission electron microscopy (TEM) images of nanopencil probes composed of a bundle of a few SWNTs with 9 nm overall diameter (a) and an individual SWNT with 3 nm diameter (b). (c) PFM height (top), amplitude (middle) and phase (bottom) images of a 50nm-thick PZT-film surface with 11.8 nm ferroelectric inverted domains formed by applying 7 V pulses to the film through the nanopencil shown in (a). (d) PFM height (top), amplitude (middle) and phase (bottom) images of the same PZT Film using the nanopencil shown in (b). No inverted domains are observed after 10 V pulses were applied.

Figures 7a,b show cross-sectional mappings of the electric field component along the polarization axis, which drives domain nucleation, under the same bias conditions as in Figures 6c,d, i.e., 7 V for the 9 nm SWNT electrode and 10 V for the 3 nm one. The white areas correspond to electric field exceeding the experimental coercive field and are a measure of inverted domain volumes. We can see that the 9 nm electrode creates a concentrated electric field underneath it that is high enough to form a fully inverted polarization domain through the entire film thickness down to the grounded electrode (Figure 7a). On the other hand, only partial inversion switching occurs for 3 nm probe (Figure 7b). For the inverted domain to remain stable, the free energy reduction rate associated with the inverted domain has to be positive (Wang & Woo, 2003; Tayebi et al., 2010a). The energy reduction rate was predicted to be positive for the case of the 9 nm SWNT electrode (Tayebi et al., 2010a). This is due to the full polarization inversion over the entire PZT thickness, which reduces the surface area and volume over which the domain wall and depolarization forces are exerted. In this case the domain wall and depolarization forces are exerted only on the sides of the inverted domain compared to being through the entire domain. Therefore, the energy reduction induced by the coercive electric field will be larger than the surface energy of the domain wall.

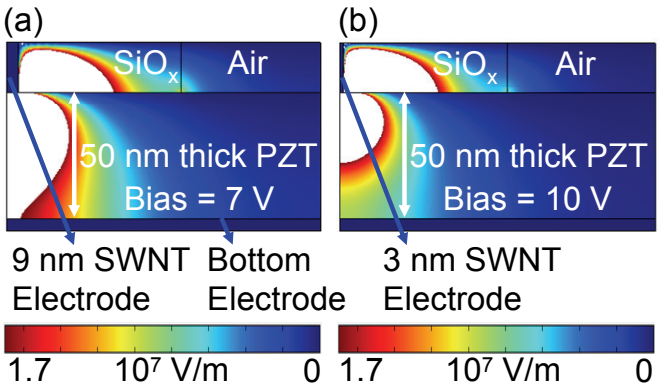

Fig. 7. (a), (b) Simulated cross-sectional mappings of the electric field component along the polarization axis under the same bias conditions of Figures 6c,d, i.e., 7 V for the 9 nm SWNT electrode (a) and 10 V for the 3 nm electrode (b) (Tayebi et al., 2010a). Due to the axial symmetry, only half of the system is shown. The white areas correspond to electric field exceeding the experimental coercive field and are a measure of inverted domain volumes.

On the other hand, the energy reduction rate was predicted to be negative for the case of the 3 nm SWNT electrode due to the partial polarization inversion (Tayebi et al., 2010a). To make the rate positive, the ferroelectric film had to be thinner to allow for full polarization inversion through the entire thicknees and therefore reduce the effects of the forces associated with domain wall and depolarization and built-in electric fields. Using a 17 nm thick PZT film, we were able to write stable 4 nm inverted domains that correpsond to 10 unit cells in size (Figure 8) (Tayebi et al., 2010a). If written in a checkerboard configuraton, densities as high as 40 Tbit/in^2 can be achieved with such small domain sizes.

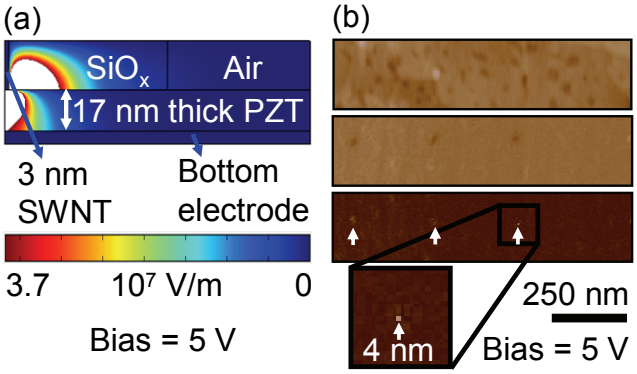

Fig. 8. Writing of stable 4 nm dots using 3 nm SWNT electrode on 17 nm thick PZT film (Tayebi et al., 2010a). (a) Simulated cross-sectional mappings of the electric field component along the polarization axis under a 5 V bias with a 3 nm SWNT electrode. Domain inversion through the entire film thickness is predicted. (b) PFM height (top), amplitude (middle) and phase (bottom) images of the 17 nm-thick PZT-film surface with 4 nm ferroelectric inverted domains formed by applying 5 V pulses to the film through the nanopencil with 3 nm electrode shown in Figure 6b.

Figure 9 depicts the minimum electrode size for predicted stable domain switching for various PZT thicknesses at different applied biases (properties of the 50 nm thick PZT film are assumed without a built-in field) (Tayebi et al., 2010a). For instance, the PZT film has to be thinner than 23 nm for a 3 nm electrode to write stable domains at 4 V bias pulses. Therefore, thinner ferroelectric films are required to enable formation of small stable domains at smaller applied biases. However, there is a critical film thickness limit below which the ferroelectric properties vanish (Junquera & Ghosez, 2003). This thickness has been estimated to be around 1.2–5 nm for both PZT (Despont et al., 2006; Fong et al., 2004; Lichtensteiger et al., 2007) and $BaTiO_3$ (Despont et al., 2006; Kim et al., 2005; Petraru et al., 2008) films. Recently, it was shown that highly strained $BaTiO_3$ films may retain their ferroelectric properties down to 1 nm thickness, i.e., below the critical thickness limit[6].

3.2 Tuning the built-in electric field

The stability of the sub-10 nm inverted domains can be further enhanced by reducing or even suppressing the built-in electric field, which is due to Pb vacancies near the surface. These vacancies are due to the high partial pressure of Pb atoms which can readily evaporate during deposition (Hau and Wong, 1995). A large remnant polarization can thus be induced, which is due to near surface concentration of trapped negative charges originating from this high vacancy density. The induced built-in electric field can exceed the coercive electric field needed for domain inversion. In such a case, stability of the inverted domains will be hard to achieve even if the forces due to depolarization charges and domain-walls are reduced. This is due to the fact that the built-in electric field is exerted over the same volume as the applied electric field, which might require a very large and impractical bias pulses to overcome the large remnant polarization. Note also that the built-in electric field is known to cause fatigue in FeRAM devices, and thus can dramatically affect the ferroelectric media lifetime (Miura & Tanaka, 1996).

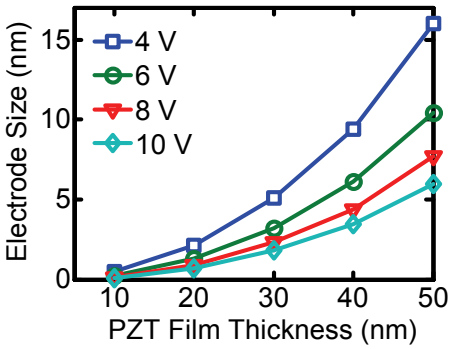

Fig. 9. Minimum electrode size for full-thickness domain inversions for various PZT thicknesses at different applied biases (Tayebi et al., 2010a).

The built-in electric-field can be tuned and suppressed by repetitive hydrogen (H_2) and oxygen (O_2) plasma treatments (Tayebit et al., submitted). Such treatments trigger reversible Pb reduction/oxidation (redox) activity, thereby altering the electrochemistry of the Pb over-layer, which compensates for charges induced by the Pb vacancies. Figure 10 shows a set of the variation of the capacitance as a function of applied bias (C–V hysteresis loop curves) before (reference curve) and after various H_2 plasma treatments, in which the pressure was varied from 0.5 to 1 torr, while the flow rate was maintained at 1000 sccm (Tayebit et al., submitted). Under such oxygen poor conditions, reduction reaction of Pb film can extract O atoms from the PZT top surface and O vacancy formation is very stable (see next section). The positive charges induced from the formation of O vacancies compensate for the already existing negative charges induced by the Pb vacancies. This, in turn, reduces (case I: 0.5 Torr pressure condition) and even suppresses (case II: 1 Torr pressure condition) the built-in electric field, making the crosspoint at 0 V (initially at 0.25 V) (Tayebit et al., submitted).

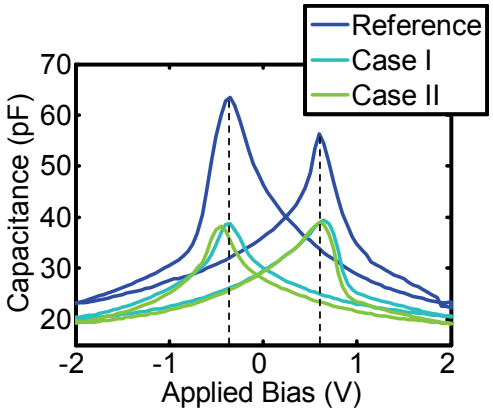

Fig. 10. Effect of the H_2 plasma treatments on the variation of capacitance as a function of applied bias. The built-in electric field decreases after each treatment, which is indicative of Pb reduction or O vacancy formation. The pressure was varied from 0.5 (case I) to 1 Torr (case II), while the gas flow rate of He with 4% H_2 was maintained at 1000 sccm (Tayebi et al., submitted).

Figure 11 shows the C–V hysteresis loop curves before (reference curve) and after the various O_2 plasma treatments, in which both pressure and gas rate where varied (Tayebit et al., submitted). Under such oxygen-rich conditions (see next section), the formation energies of O vacancies are highly positive and are thus unstable. The O_2 plasma treatments oxidize Pb in the PZT film, thereby filling the O vacancies that might have already existed in the film. This leads to an increase of negative charges induced by the Pb vacancies, which in turn shifts the C–V curve and hence increases the built-in electric field. Increasing the pressure and gas flow increases further the built-in electric field, thereby exacerbating its effect (case III to case IV).

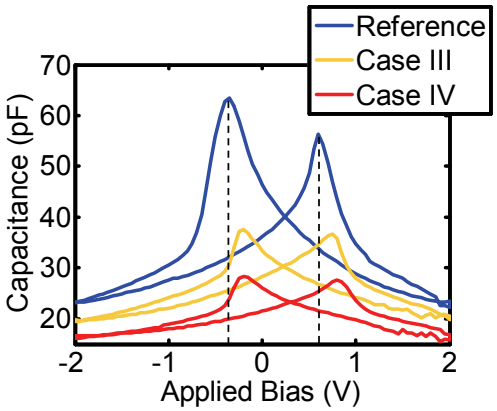

Fig. 11. Effect of the O2 plasma treatments on C–V hysteresis loop curve. The built-in electric field increases after each treatment, which is indicative of Pb oxidation or O vacancy filling. The O2 flow rate and pressure were varied from 100 sccm and 0.5 Torr (case III) to500 sccm and 5 Torr, respectively (Tayebi et al., submitted).

3.3 Review of a*b-Initio* studies of vacancy formation in PZT films

The formation of defects including lead vacancies $\left(V_{Pb}^{-2}\right)$ and O vacancies $\left(V_{O}^{+2}\right)$ under oxygen rich (oxidizing environment) and oxygen poor (reducing environment) has recently been investigated theoretically using *ab-initio* studies for $PbTiO_3$ (Zhukovskii et al., 2009; Zhang et al. 2006; Zhang et al., 2008) and $PbZrO_3$ (Zhukovskii et al., 2009). Note that $PbTiO_3$ and $PbZrO_3$ are the two systems that compose the PZT material. Moreover, besides Pb, Ti and Zr vacancies, there are two types of O vacancies that need to be taken into account. These correspond to O atoms bound to Ti/Zr in the *z* direction referred to as O1, and O atoms bound to Ti/Zr in *x*-*y* plane referred to as O2 (Figure 12). These calculations shed light on the charge compensation mechanism that enables the tuning of the built-in electric field and are thus reviewed here.

Figure 13a shows the variation of formation energies of various vacancies under oxygen-rich (oxidizing) conditions (Zhang et al. 2006). The formation energies of Pb vacancies are negative throughout the band gap of the PZT material. This confirms that the formation of Pb vacancies is an exothermic and spontaneous process that can happen during film growth. This is in agreement with our experimental observations where we attributed the origin of the built-in electric field and *p*-type conduction to the formation of Pb vacancies. On the other

hand, no O vacancies are stable given their highly positive formation energy. Therefore, under the oxygen rich conditions, the Pb vacancies cannot be compensated for. In fact, any O and Pb vacancies that might have been present will be filled by O atoms thereby oxidizing Pb. Such mechanism will exacerbate the effect of the built-in electric field and will increase the acceptor doping density. Note that Ti vacancies also possess very highly positive formation energies and are not susceptible to form. Although not shown in Figure 13a, this is also the case of Zr as reported in other *ab-initio* studies (Zhukovskii et al., 2009).

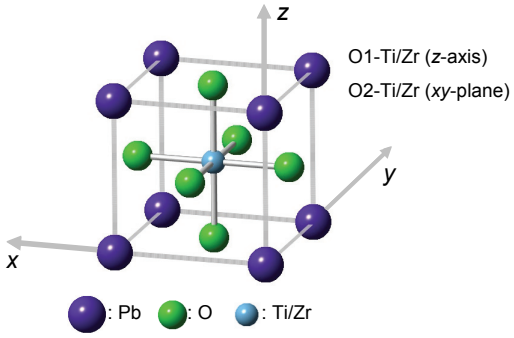

Fig. 12. PZT unit cell depicting the two types of O atoms. O atoms bound to Ti/Zr in the z direction are referred to as O1, and O atoms bound to Ti/Zr in x-y plane are referred to as O2.

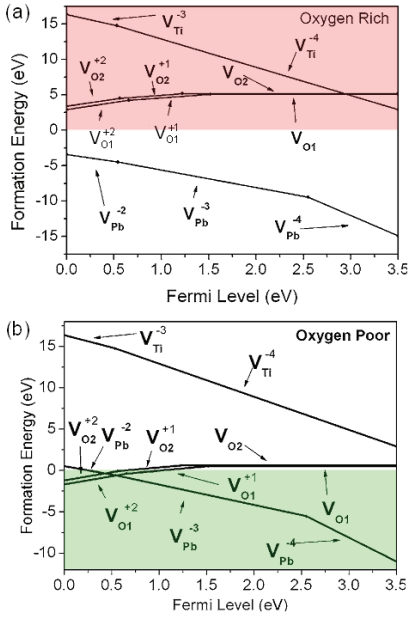

Fig. 13. Previously published *ab-initio* calculations of defect formation energy for vacancies as a function of the Fermi level in oxygen-rich (a) and oxygen-poor (b) conditions (Zhang et al., 2006). Only the vacancies among the lowest formation energies are shown.

On the other hand, both O and Pb vacancies possess negative formation energies under the oxygen-poor (reducing) conditions, as shown in Figure 13b (Zhang et al., 2006). Therefore both vacancies are susceptible to form under these conditions. Moreover, the V_O^{+2} vacancy possesses even lower formation energy than V_{Pb}^{-2} at the same Fermi level, and is thus more stable. Therefore, the large density of the O vacancies under oxygen poor conditions will affect the initial *p*-type conductivity of the PZT film. It will also reduce, suppress or even change the direction of the built-in electric field if the O vacancies exceed the Pb ones.

4. Probe-based reading techniques

A few conventional probe-based reading techniques have been developed and that are capable of detecting polarization bit signals at the required high scanning speeds on the order of mm/s which are required for high data access rates (Nath et al., 2008; Hiranaga et al., 2007; Park et al., 2004). However, not all techniques are suitable for a MEMS-based probe storage system. For example, piezoresponse force microscopy (PFM) (Tybell et al., 1998; Hong et al., 2002; Kalinin et al., 2004; Nath et al., 2008) uses an opto-electro-mechanical setup to detect high-frequency piezoactuation signals while scanning without active tracking of surface to achieve high-speed imaging of local polarizations (Nath et al., 2008). This is achieved by measuring the mechanical response of the ferroelectric film when an AC voltage is superimposed to the surface during scanning. In response to the electrical stimulus (inverse piezoelectric effect), the film locally expands or contracts inducing a deflection of the probe-cantilever, which is measured using a split photodiode detector, which is then demodulated. The piezoelectric response of the sample is the first harmonic component of the bias induced tip deflection *z*. When a bias $V = V_{DC} + V_{AC}\cos(\omega t)$ is applied to the probe-tip, the resulting cantilever deflection $z = z_{DC} + A(\omega, V_{DC}, V_{AC})\cos(\omega t + \phi)$, where A and φ are the amplitude and phase of the electromechanical response, respectively. For down polarized domains, the application of a positive tip-bias results in sample expansion, and surface oscillations are in phase with the applied bias, i.e., $\varphi = 0$. On the other hand, the surface oscillations are out of phase with the applied bias for up polarized domain, and the phase is shifted by 180°. There are other techniques that are exclusively electrically-based such as scanning nonlinear dielectric (Hiranaga et al., 2007) and scanning resistive probe (Park et al., 2004) microscopy techniques. However, these two techniques require complex configurations such as the use of a coaxial tip geometry to allow for fast reading of capacitance changes associated with polarization domain signals, and field effect sensors integrated at the tip apex, respectively.

Recently, a technique called charge-based scanning probe read-back microscopy has been developed (Forrester et al, 2009). In this technique, ferroelectric inverted domains are read back destructively by applying a constant voltage of magnitude greater than the coercive voltage needed for polarization reversal. This is similar to FeRAM-based reading mechanism. In this process, the flow of screening charges through the read-back amplifier provides sufficient signal to enable the read of inverted domains as small as 10 nm with frequencies read-back at rates as high as 1.5 MHz and speeds as high as 2 cm/s, which is much faster than other developed techniques. Figure 14 shows the reading mechanism used in this technique. During scanning, a constant voltage is applied between the moving tip and the bottom electrode on which the ferroelectric film is deposited. This in turn causes

inverted domains whose polarization direction is anti-parallel to the applied electric field to invert back. This causes the bound charge at the top and bottom surfaces to reverse and thus the surface screening charges also reverse. The resulting charge flow can be detected by a charge- or current-sensitive amplifier. Knowing what the film polarization is, the inverted domain area can be determined from the detected charge signal. Figure 15 shows a read-back signal for a single tone pattern of inverted domains in which switching and non-switching signals are resolved with high signal-to-noise ratio. The main disadvantage of this technique, however, is that the reading is destructive and requires immediate rewriting of bits, which can cause rewriting inaccuracies from probe registry offsets. It can also induce slower access rates.

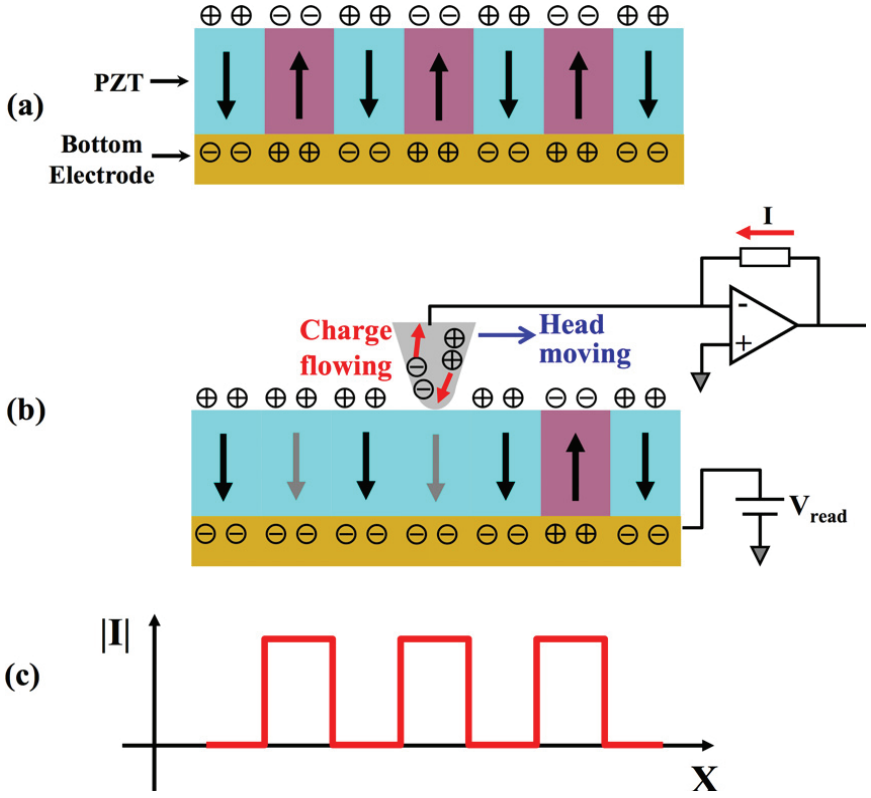

Fig. 14. Schematic drawing of the ferroelectric read-back process (Forrester et al., 2009). (a) A domain pattern of alternating up and down polarizations. The circled symbols represent screening charges which compensate the bound charges associated with each polarization. (b) During read-back a constant voltage is applied between the probe tip and the base electrode causes reversal (erasing) of domains whose polarization is opposite to the applied electric field. The resulting flow of screening charges is sensed by the read-back amplifier, producing a read-back signal that is schematically shown in (c).

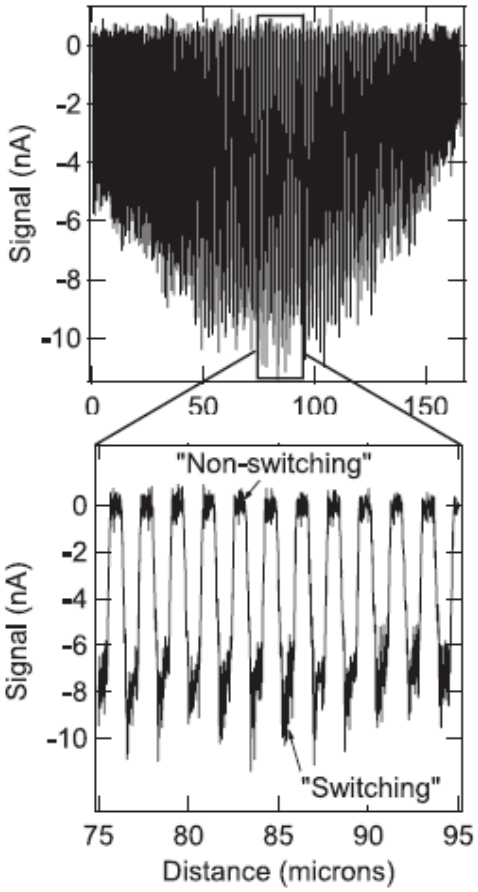

Fig. 15. Read-back data of a 800 nm bit length, showing an entire 170 μm track (Forrester et al., 2009).

Another recently developed technique, which has the advantage of using a nondestructive read process, is the scanning probe charge reading technique (Kim et al., 2009). Unlike the PFM technique, this technique uses the direct piezoelectric effect. The applied normal force excreted by the probe-tip during scanning causes a charge buildup Q related to the force by the equation $Q=d_{33}F$, where d_{33} is a piezoelectric coefficient of the ferroelectric medium along the polarization access. Therefore, a current is generated due to a change in charge when the probe tip crosses a domain wall of the inverted domain. The sign of the current depends on whether the probe tip moves from an up to down polarization or vice versa. Figure 16 shows a schematic of the operational principle of this technique in which a series of inverted domains written with wavelength λ are read using this technique. By converting the charge coupled to the probe tip from the ferroelectric film into an output voltage, the desired alternating polarization charges are read. The voltage signal is fed through a band- pass filter to generate a cleaner signal, V_{BPF}.

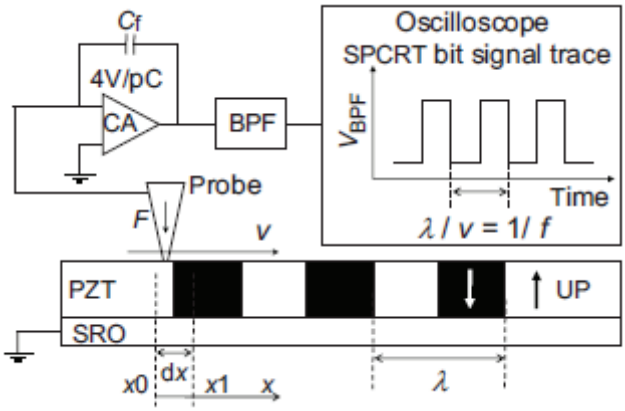

Fig. 16. Schematic drawing of the principle of operation and a test setup of the scanning probe charge reading technique to read ferroelectric bits (Kim et al., 2009).

Figure 17 shows a set of voltage signal traces corresponding to three inverted-domain wavelengths: 1.6, 1.2, and 0.8 μm, respectively and for various applied forces at a scanning speed of 1.6 mm/s. The signal-to-noise ratio for the three wavelengths increases from 14, 12, and 10 dB to 17, 15, and 13 dB as the applied force is increased from 100 nN to 800 nN. When the probe tip is disengaged no discernable signal is detected.

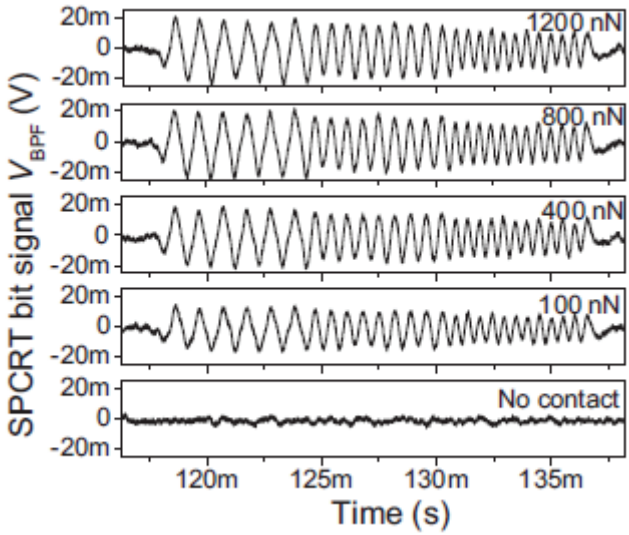

Fig. 17. Bit signal traces in time domain of the three different wavelengths (1.6, 1.2, and 0.8 μm), alternating polarizations at various applied forces. The scanning speed was maintained at 1.6 mm/s (Kim et al., 2009).

5. A 5 kilometer tip-wear endurance mechanism

For probe-based memory devices to be technologically competitive, the write and read operations have to be achieved at high access rates with sliding velocities on the order of 5 to 10 mm/s, over a lifetime of 5 to 10 years, corresponding to probe-tip sliding distances of 5 to 10 km. The bit size, and thus the storage density, mainly depends on the radius of the probe-tip, which is prone to rapid mechanical wear and dulling due to the high-speed contact mode operation of the system (Cho et al., 2006; Knoll et al., 2006; Bhushan et al., 2008; Gotsmann & Lantz, 2008). This tip wear can cause serious degradation of the write-read resolution over the device lifetime and remains the most important fundamental issue facing probe-based storage.

In principle, the tip wear rate could be reduced by using hard conductive diamond coatings (Cho et al., 2006). However, such coatings are usually deposited at high temperatures (~900^{o}C), which are not compatible with integration processes of on-chip electronic circuits (Heck et al., 2010). The diamond coatings are also very rough and have to be sharpened by focus ion beam schemes to reduce the tip radius in order to achieve the required write-read resolution (Cho et al., 2006), which make it difficult for large scale batch fabrication of probe arrays (Heck et al., 2010). Carbon nanotube probe-tips, which due to their cylindrical shape can retain their write-read resolution even after significant wear, have also been proposed. These include "naked" carbon nanotube probes (Lantz et al., 2003) and the dielectric-sheathed carbon nanotube probes presented in section 3 (Tayebi et al., 2010a). It will, however, take a significant time and research effort to bring such probes to large scale fabrication (Heck et al., 2010). Thus conventional conductive coatings with small tip radius that can be deposited at ambient or low temperature conditions, such as platinum-iridium (PtIr), remain the best choice at the present time.

Our group has developed a scheme for a wear endurance mechanism which allows a conductive PtIr coated probe-tip sliding over a ferroelectric film at a 5 mm/s velocity to retain its write-read resolution over a 5 km distance, which corresponds to a 5 year device lifetime (Tayebi et al., 2010b). This mechanism was achieved by sliding the probe-tip at low applied forces on atomically smooth surfaces with force modulation and in the presence of thin water films under optimized humidity. Under the conditions of low applied forces on atomically smooth surfaces, the adhesive elastic wear regime is dominant, whereas the abrasive wear regime encountered in rough contact is significantly reduced. This in turn reduces the wear rate by orders of magnitude. In the elastic wear regime, the wear volume is inversely dependent on the elastic modulus of the coating rather than its hardness (Bhushan, 2002).

Modulating the force in the presence of an ultrathin water layer, which acts as a viscoelastic film, further reduced the wear volume to insignificant amounts. This is because force modulation enables the probe-tip to recover elastically during sliding every time the nominal force is reduced during a modulation cycle. This in turn would relax the stress level on bonds between atoms that are taking part in the wear process, delay bond breaking, and thus reduce wear. Furthermore, the insertion of the ultrathin water film that is a few monolayers in thickness at the tip-sample interface provides further wear rate reduction. Such a thin film strongly adheres to the surface, thus forming a liquid crystal, and is not energetically favored to form a meniscus at the tip-sample interface.

Under force modulation of high frequency, this water film can act as a viscoelastic material, which would further reduce the stress level on such bonds and decrease friction and wear.

Figures 18b,c show SEM images of the PtIr probe-tip after 2.5 km and 5 km sliding distances (corresponding to two weeks of continuous sliding) under the conditions mentioned above. The wear volume is estimated to be 3.32×10^3 nm^3 after 2.5 km and 5.6×10^3 nm^3 after 5 km. Figures 18d,e show a 3×1 matrix of inverted domain dots written by applying 100 μs wide pulses of 5V before and after 5 km sliding, with the same domain sizes of 15.6 nm. Although the tip has shown a small amount of wear, the write and read resolutions were therefore not lost after 5 km of sliding at 5 mm/s.

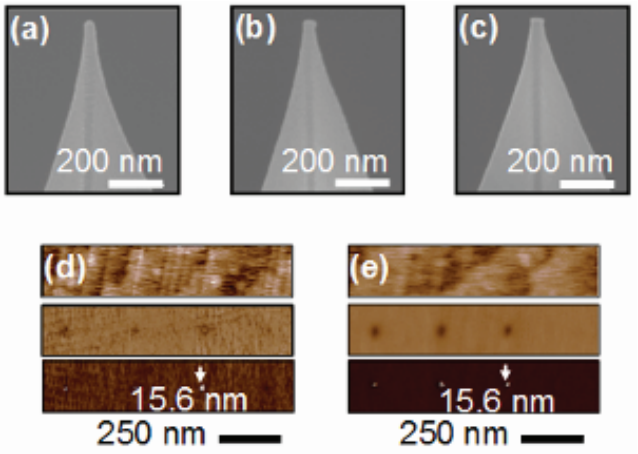

Fig. 18. Wear tests on PtIr probe-tips sliding over a PZT surface with 0.17 nm RMS roughness with force modulation and water lubrication (Tayebi et al., 2010b). (a-c) SEM images of as received PtIr probe-tip prior to sliding (a), after 2.5 km (b) and 5 km (c) of sliding at 5 mm/s with an applied normal force F_N = 7.5 nN that is modulated at 200 kHz. (d, e) PFM height (top), amplitude (middle) and phase (bottom) images of the PZT-film surface with 3×1 matrix of 15.6 nm inverted domains formed by applying 100 μs pulses of 5 V using the probe-tip prior to (d) and after (e) the 5 km sliding experiment.

On the other hand, sliding experiments performed without force modulation while keeping other conditions identical including the 25% RH level, showed a significant tip blunting after only 500 m sliding with a tip wear volume of 8.2×10^5 nm^3 (Figures 19a,b). Figures 19c,d show a 4×1 matrix of inverted domain dots written by applying 100 μs wide pulses of 5V before and after the 500 m sliding. Here the dot size increased by 31.4 nm from the as-received tip conditions. Therefore sliding under force modulation within the elastic adhesive wear regime and in the presence of a thin water layer greatly reduces wear. These results could lead to parallel-probe based data storage devices that exceed the capabilities of current hard drive and solid state disks given the ultrahigh density capabilities. It can also allow other scanning probe based systems such as AFM-based lithograph.

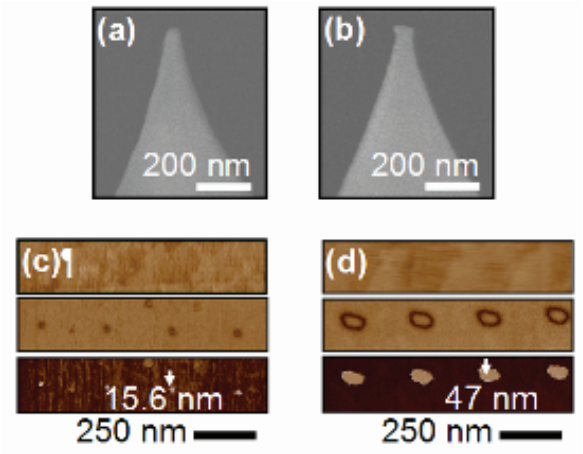

Fig. 19. Wear tests on PtIr probe-tips sliding over a PZT surface with 0.17 nm RMS roughness without force modulation (Tayebi et al., 2010b). (a, b) SEM images of another PtIr probe-tip prior (a) and after 500 m (b) of sliding at 5 mm/s with an applied normal force F_N = 7.5 nN without force modulation. (c) Height (top), amplitude (middle) and phase (bottom) images of the film surface with 4×1 matrix of 15.6 nm inverted domains formed under the same conditions using the PtIr probe-tip prior to the 500 m sliding experiment without modulation. (d) Height (top), amplitude (middle) and phase (bottom) images of the film surface with 4×1 matrix of 47 nm inverted domains formed under the same conditions after the 500 m sliding experiment. The size of the inverted domains increased by 31.2 nm after sliding.

6. Conclusions

This chapter reviewed recent progress to address several fundamental issues that have remained a bottleneck for the development and commercialization of ultrahigh density probe-based nonvolatile memory devices using ferroelectric media, including stability of sub-10 nm inverted ferroelectric domains, reading schemes at high operating speeds compatible with MEMS-based storage systems, and probe-tip wear.

Stable inverted domains less than 10 nm in diameter could be formed in ferroelectric films when inversion occurred through the entire ferroelectric film thickness. Polarization inversion was found to depend strongly on the ratio of the electrode size to the ferroelectric film thickness. This is because full inversion minimized the effects of domain-wall and depolarization energies by reducing the domain sidewalls and, thus enabling positive free energy reduction rates. With this understanding, stable inverted domains as small as 4 nm in diameter were experimentally demonstrated. Moreover, the reduction and suppression of the built-in electric field, which would enhance the stability of sub-10 nm domains in up and down-polarized ferroelectric PZT films, could be achieved by repetetive O_2 and H_2 plasma treatments to oxidize/reduce the PZT surface, thereby altering the electrochemistry of the Pb over-layer. These treatments compensate for the negative charges induced by the Pb vacancies that are at the origin of the built-in electric field.

Two probe-based reading techniques have shown potential compatibility with MEMS-based probe storage systems at high speed rates: the charge-based scanning probe and the

scanning probe charge reading techniques. In the charge-based scanning probe read-back microscopy, ferroelectric inverted domains are read back destructively by applying a constant voltage that is greater than the coercive voltage of the ferroelectric film. In this process, the flow of screening charges through the read-back amplifier provides sufficient signal to enable the read of inverted domains as small as 10 nm with frequencies read-back at rates as high as 1.5 MHz and speeds as high as 2 cm/s. For the case of the scanning probe charge reading technique, the direct piezoelectric effect is used. The applied normal force excreted by the probe-tip during scanning causes a charge buildup, which generates a current when the probe tip travels across a domain wall of the inverted domain. Besides reading at high speeds, this technique has the advantage of being nondestructive.

Lastly, we discussed a wear endurance mechanism which enabled a conductive PtIr coated probe-tip sliding over a ferroelectric film at a 5 mm/s velocity to retain its write-read resolution over a 5 km distance, corresponding to 5 years of device lifetime. This was achieved by sliding the probe-tip at low applied forces on atomically smooth surfaces, with force modulation, and in the presence of thin water films under optimized humidity. Under the conditions of low applied forces on atomically smooth surfaces, the adhesive elastic wear regime was dominant, and the wear rate was reduced by orders of magnitude. In this regime, the wear volume is inversely dependent on the elastic modulus of the coating rather than its hardness. Modulating the force in the presence of a thin water layer, which acts as a viscoelastic film, further reduced the wear volume to insignificant amounts.

The novel solutions summarized in this chapter could lead to parallel-probe based data storage devices that exceed the capabilities of current hard drive and solid state disks given the ultrahigh density capabilities this technology possesses. While fundamental issues have been addressed, the solutions were obtained at the single probe level. Therefore, these solutions have to be tested and validated in actual devices, such as the Intel's SSP memory device (Heck et al., 2010) where 5000 MEMS cantilever-probes can simultaneously perform write and read operations.

7. References

Ahn, C. H., Tybell, T., Antognazza, L., Char, K.; Hammond, R. H., Beasley, M. R.; Fischer, Ø., and Triscone J.-M. (1997). Nonvolatile electronic writing of epitaxial $Pb(Zr_{0.52}Ti_{0.48})O_3/SrRuO_3$ heterostructures, *Science*, Vol. 276, pp. 1100.

Ahn, C. H., Rabe, M. R., and Triscone, J.-M. (2004). Ferroelectricity at the nanoscale: Local polarization in oxide thin films and heterostructures, *Science*, Vol. 303, pp. 488.

Bhushan, B., Kwak, K. J., and Palacio, M. (2008). Nanotribology and nanomechanics of AFM probe-based data recording technology, *Journal of Physics: Condensed Matter*, Vol. 20, pp. 365207.

Bhushan, B. (2002). *Introduction to Tribology*. New York, NY. John Wiley & Sons.

Cho, Y., Fujimoto, K., Hiranaga, Y., Wagatsuma, Y., Onoe, A., Terabe, K., and Kitamura, K. (2003). Terabit/inch^2 ferroelectric data storage using scanning nonlinear dielectric microscopy nanodomain engineering system, *Nanotechnology,* Vol. 14, pp. 637.

Cho, Y., Hashimoto, S., Odagawa, N., Tanaka, K., and Hiranaga, Y. (2005). Realization of 10 Tbit/in^2 memory density and subnanosecond domain switching time in ferroelectric data storage, *Applied Physics Letters* Vol. 87, pp. 232907.

Cho, Y., Hashimoto, S., Odagawa, N., Tanaka, K., and Hiranaga, Y. (2006). Nanodomain manipulation for ultrahigh density ferroelectric data storage, *Nanotechnology,* Vol. 17, pp. S137.

Despont, L., Koitzsch, C., Clerc, F.; Garnier, M. G., Aebi, P., Lichtensteiger, C., Triscone, J.-M., Garcia de Abajo, F. J., Bousquet, E. and Ghosez, Ph. (2006). Direct evidence for ferroelectric polar distortion in ultrathin lead titanate perovskite films, *Physical Review B*, Vol. 73, pp. 094110.

Fong, D. D., Stephenson, G. B., Streiffer, S. K., Eastman, J. A., Auciello, O., Fuoss, P. H. and Thompson, C. (2004). Ferroelectricity in ultrathin perovskite films, *Science*, Vol. 304, pp. 1650.

Forrester, M. G., Ahner, J. W., Bedillion, M. D., Bedoya, C., Bolten, D. G., Chang, K-C, de Gersem, G., Hu, S., Johns, E. C., Nassirou, M., Palmer, J., Roelofs, A., Siegert, M., Tamaru, S., Vaithyanathan, V., Zavaliche, F., Zhao, T., and Zhao Y. (2009). Charge-based scanning probe readback of nanometer-scale ferroelectric domain patterns at megahertz rates, *Nanotechnology* Vol. 20,pp. 225501.

Garcia, V., Fusil, S., Bouzehouane, K., Enouz-Vedrenne, S., Mathur, N. D., Barthélémy, A. and Bibes, M. (2009). Giant tunnel electroresistance for non-destructive readout of ferroelectric states, *Nature*, Vol. 460, pp. 81.

Gotsmann, B. and Lantz, M. A. (2008). Atomistic wear in a single asperity sliding contact, *Physical Review Letters,* Vol. 101, pp. 125501.

Hamann, H., O'Boyle, M., Martin, Y. C., Rooks, M., and Wickramasinghe, H. K. (2006). Ultra-high-density phase-change storage and memory, *Nature Materials,* Vol. 5, pp. 383.

Hau, S.K. and Wong, K.H. (1995). Intrinsic resputtering in pulsed–laser deposition of lead–zirconate–titanate thin films, *Applied Physics Letters*, Vol. 66, pp. 245.

Heck, J., Adams, D., Belov, N., Chou, T. A., Kim, B., Kornelsen, K., Ma, Q., Rao, V., Severi, S., Spicer, D., Tchelepi, G. and Witvrouw, A. (2010). Ultra-high density MEMS probe memory device, *Microelectronic Engineering*, Vol. 87, pp. 1198.

Hiranaga, Y., Uda, T. Kurihashi, Y., Tanaka, K. and Cho, Y. (2007). Novel HDD-type SNDM ferroelectric data storage system aimed at high-speed data transfer with single probe operation. *IEEE Transanctions on Ultrasonnics,.Ferroelectrics and Frequency Control*, Vol. 54, pp. 2523.

Junquera, J. and Ghosez, P. (2003). Critical thickness for ferroelectricity in perovskite ultrathin films, *Nature*, Vol. 422, pp. 506.

Hong, S., Shin, H., Woo, J. and No, K. (2002). *Effect of cantilever–sample interaction on piezoelectric force microscopy, Applied Physics Letters,* Vol. 80, pp. 1453

Kalinin, V., Karapetian, E. and Kachanov, M. (2004). Nanoelectromechanics of piezoresponse force microscopy, *Physical Review B,* Vol. 70, pp. 184101.

Kim, B. M, Adams, D. E., Tran, Q., Ma, Q. and Rao, V. (2009). Scanning probe charge reading of ferroelectric domains, *Applied Physics Letters*, Vol. 94, pp. 063105.

Kim, D. J., Jo, J. Y., Kim, Y. S., Chang, Y. J., Lee, J. S., Yoon, J. G., Song, T. K. and Noh, T. W. (2005). Polarization relaxation induced by a depolarization field in ultrathin ferroelectric $BaTiO_3$ capacitors, *Physical Review Letters*, Vol. 95, pp. 237602.

Knoll, A., Bächtold, P., Bonan, J., Cherubini, G., Despont, M., Drechsler, U., Dürig, U., Gotsmann, B., Häberle, W., Hagleitner, C., Jubin, D., Lantz, M.A., Pantazi, A., Pozidis, H., Rothuizen, H., Sebastian, A., Stutz, R., Vettiger, P., Wiesmann D. and

Eleftheriou, E.S. (2006). Integrating nanotechnology into a working storage device," *Microelectronics Engineering,* Vol. 83, pp. 1692.

Kim, Y. S ., Kim, D. H., Kim, J. D., Chang, Y. J., Noh, T. W., Kong, J. H., Char, K., Park, Y. D., Bu, S. D., Yoon, J.-G. and Chung, J.-S. (2005). Critical thickness of ultrathin ferroelectric $BaTiO_3$ films, *Applied Physics Letter*s, Vol. 86, pp. 102907.

Lantz, M. A., Gotsmann, B., Durig, U. T., Vettiger, P., Nakayama, Y., Shimizu, T. and Tokumoto, H. (2003). Carbon nanotube tips for thermomechanical data storage, *Applied Physics Letter,* Vol. 83, pp. 1266.

Lichtensteiger, C., Dawber, M., Stucki, N., Triscone, J.-M., Hoffman, J., Yau, J.-B., Ahn, C. H., Despont, L. and Aebi, P. (2007). Monodomain to polydomain transition in ferroelectric $PbTiO_3$ thin films with $La_{0.67}Sr_{0.33}MnO_3$ electrodes, *Applied Physics Letters*, Vol. 90, pp. 052907.

Li, X., Mamchik, A. and Chen, I.-W. (2001). Stability of electrodeless ferroelectric domains near a ferroelectric dielectric interface, *Applied Physics Letters,* Vol. 79, pp. 809.

Miura, K. and Tanaka M, (1996). Origin of Fatigue in Ferroelectric Perovskite Oxides, *Japanese Journal of Applied Physics*, Vol. 35, pp. 2719.

Nath, R., Chu, Y. –H, Polomoff, N. A., Ramesh, R., and Huey, B. D. (2008). High speed piezoresponse force microscopy: <1 frame per second nanoscale imaging, *Applied Physics Letters*, Vol. 93, pp. 072905.

Pantazi, A., Sebastian, A., Antonakopoulos, T. A., Bächtold, P., Bonaccio, A. R., Bonan, J., Cherubini, G., Despont, M., DiPietro, R. A., Drechsler, U., Dürig, U., Gotsmann, B., Häberle, W., Hagleitner, C., Hedrick, J. L., Jubin, D., Knoll, A., Lantz, M. A., Pentarakis, J., Pozidis, H., Pratt, R. C., Rothuizen, H., Stutz, R., Varsamou, M., Wiesmann, D., and Eleftheriou, E., (2008). Probe-based ultrahigh-density storage technology, *IBM Journal of Research and Development, Vol. 52*, pp. 493.

Park, H., Jung, J., Min, D. -K., Kim, S., Hong, S. and Shin, H. (2004). Scanning resistive probe microscopy: Imaging ferroelectric domains. *Applied Physics Letters,* Vol. 84, pp. 1734.

Petraru, A., Kohlstedt, H., Poppe, U., Waser, R., Solbach, A., Klemradt, U., Schubert, J., Zander, W. and Pertsev, N. A. (2008). Wedgelike ultrathin epitaxial $BaTiO_3$ films for studies of scaling effects in ferroelectrics, *Applied Physics Letters*, Vol. 93, pp. 072902.

Tayebi, N., Nauru, Y., Franklin, N., Collier, C. P., Giapis, K. P., Nishi, N., and Zhang, Y. (2010). Fully Inverted Single-Digit Nanometer Domains in Ferroelectric Films, *Applied Physics Letters*, Vol. 96, No. 2, pp. 023103.

Tayebi, N., Narui, Y., Chen, R. J., Collier, C. P., Giapis, K. P., and Zhang, Y. (2008a). Nanopencil as a Wear-Tolerant Probe for Ultrahigh Density Data Storage, Applied Physics Letters, Vol. 93, No. 10, pp. 103112.

Tayebi, N., Zhang, Y., Chen, R. J., Tran, Q., Chen, R., Ma, Q., Nishi, Y., and Rao, V. (2010b) An Ultraclean Tip-Wear Reduction Scheme for Ultrahigh Density Scanning Probe-Based Data Storage, *ACS NANO,* Vol. 4, No. 10, pp. 5713-20.

Tayebi, N., Kim, S., Franklin, N., Chen, R..J., Tran, Q., Ma, Q., Nishi, Y., and Rao, V. (submitted). Tuning and Suppression of Built-in Electric Field for Long Term Retention of Single-Digit Nanometer Domains in Ferroelectric Films.

Tybell, T., Ahn, C. H. and Triscone, J. -M. (1998). Control and imaging of ferroelectric domains over large areas with nanometer resolution in atomically smooth epitaxial Pb(Zr0.2Ti0.8)O3 thin films. *Applied Physics Letters*, Vol. 72, pp. 1454.

Vettiger, P., Cross, G., Despont, M., Drechsler, U., Dürig, U., Gotsmann, B., Häberle, W., Lantz, M. A., Rothuizen, H. E., Stutz, R., and Binnig G. K. (2002). The 'Millipede' – Nanotechnology entering data storage, *IEEE Transactions on Nanotechnology*, Vol. 1, pp.

Wang, B. and Woo, C.H. (2003). Stability of 180° domain in ferroelectric thin films, *Journal of Applied Physics*, Vol. 94, pp. 610.

Zhang, Z., Wu, P., Lu, L. and Shu, C. (2006). Study on vacancy formation in ferroelectric $PbTiO_3$ from *ab initio*, *Applied Physics Letters* Vol. 88, pp. 142902.

Zhang, Z., Wu, P., Lu, L. and Shu, C. (2008). *Ab initio* study of formations of neutral vacancies in ferroelectric $PbTiO_3$ at different oxygen atmospheres, *Journal of Alloys and Compounds Vol. 449*, pp. 362.

Zhukovskii, Y. F., Kotominb, E. A., Piskunov, S. and Ellis, D.E., (2009). A comparative *ab initio* study of bulk and surface oxygen vacancies in $PbTiO_3$, $PbZrO_3$ and $SrTiO_3$ perovskites, *Solid State Communications,* Vol. 149, pp. 1359.

8

Fabrication and Study on One-Transistor-Capacitor Structure of Nonvolatile Random Access Memory TFT Devices Using Ferroelectric Gated Oxide Film

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1. Introduction

Recently, non-volatile and volatile memory devices such as static random access memory (SRAM), dynamic random access memory (DRAM), Flash memory, EPROM and E^2PROM were very important for applications in conventional personal computer and micro-processor, and performance efficiency of hardware improved by their low voltage, high operation speed, and large storage capacity. The non-volatile memory devices were widely investigated and discussed among these memory devices. Many kind of the non-volatile memory device were ferroelectric random access memory (FeRAM), magnetron random access memory (MRAM), and resist random access memory (RRAM) devices. Up to now, the non-volatile ferroelectric random access memory (FeRAM) devices were attractive because of their low coercive filed, large remnant polarization, and high operation speed among various non-volatile access random memory devices [1].

The non-volatile FeRAM devices were limited by their relative larger one-transistor-one-capacitor (1T-1C) size. Thus, one-transistor-capacitor (1TC) structure ferroelectric memory was desirable because of the better sensitivity and small size than 1T-1C structure ferroelectric memory [2-4]. The operation characteristics and reliability of ferroelectric capacitor structure of 1T-1C memory cell were spending lots cost during the fabrication process.

In addition, electronic devices and system-on-panel (SOP) technology were widely discussed and researched. For SOP concept, the switch characteristics of various thin-film transistor (TFT) structures were widely investigated for applications in amorphous silicon (α-Si) and polycrystal silicon (poly-Si) active matrix liquid-crystal-display (AM-LCD) displays [5-7]. Integrated electron devices such as memory devices, control devices, and central processing units (CPU) on transparent conductive thin films will be important in the future. The excellent electrical, physical, and reliability characteristics of metal-ferroelectric-metal (MFM) capacitor structures for 1T1C memory cells were enhanced using transparent conductive thin films on glass substrates.

2. Electrical properties of non-volatile RAM using ferroelectric thin film

S. Y. Wu firstly reported that an MFS transistor fabricated by using bismuth titanate in 1974 [2-3]. The first ferroelectric memory device was fabricated by replacing the gate oxide of a conventional metal-oxide-semiconductor (MOS) transistor with a ferroelectric material. However, the interface and interaction problem between the silicon substrate and ferroelectric films were very important factors during the high temperature processes in 1TC structure. To overcome the interface and interaction problem, the silicon dioxide and silicon nitride films were used as the buffer layer. The low remnant polarization and high operation voltage of 1TC were also be induced by gate oxide structure with double-layer ferroelectric silicon dioxide thin films. Sugibuchi et al. provided a 50 nm silicon dioxide thin film between the $Bi_4Ti_3O_{12}$ layer and the silicon substrate [8].

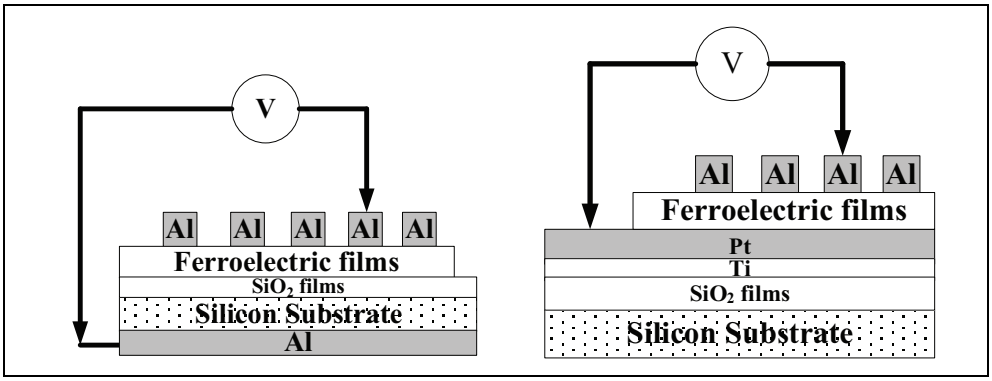

Fig. 1. (a) Metal-ferroelectric-insulator-semiconductor (MFIS) structure, and (b) Metal ferroelectric-metal (MFM) structure.

The ferroelectric ceramic target prepared, the raw materials were mixed and fabricated by solid state reaction method. After mixing and ball-milling, the mixture was dried, grounded, and calcined for some time. Then, the pressed ferroelectric ceramic target with a diameter of two inches was sintered in ambient air. The base pressure of the deposited chamber was brought down 1×10^{-7} mTorr prior to deposition. The target was placed away from the $Pt/Ti/SiO_2/Si$ and SiO_2/Si substrate. For metal-ferroelectric-metal (MFM) capacitor structure, the Pt and the Ti were deposited by dc sputtering using pure argon plasma as bottom electrodes. The SiO_2 thin films were prepared by dry oxidation technology. The metal-ferroelectric-insulator-semiconductor (MFIS) and metal-ferroelectric-metal (MFM) structures were shown in Fig. 1.

For the physical properties of ferroelectric thin films obtained, the thickness and surface morphology of ferroelectric thin films were observed by field effect scanning electron microscopy (FeSEM). The crystal structure of ferroelectric thin films were characterized by an X-ray diffraction (XRD) measurement using a Ni-filtered CuKα radiation. The capacitance-voltage (C-V) properties were measured as a function of applied voltage by using a Hewlett-Packard (HP 4284A) impedance gain phase analyzer. The current curves versus the applied voltage (I-V characteristics) of the ferroelectric thin films were measured by a Hewlett-Packard (HP 4156) semiconductor parameter analyzer.

Additionally, the ferroelectric thin films were used in a one-transistor-capacitor (1TC) structure of the amorphous-Si TFT device to replace the gate oxide of random access memory devices. For that, a bottom-gate amorphous thin-film transistor, as shown in Fig.2, would be fabricated and the characteristics of the fabricated devices were successfully developed.

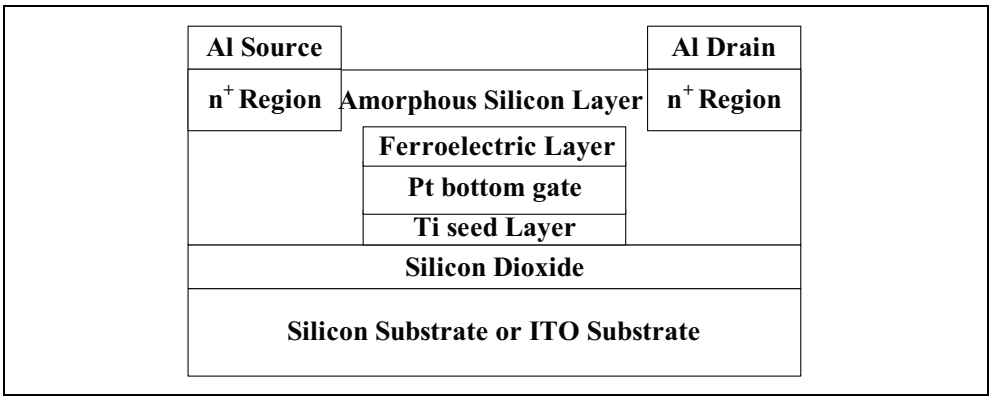

Fig. 2. The 1TC FeRAM device fabricated with ferroelectric thin film.

For 1TC FeRAM device fabricated, a one-transistor-capacitor (1TC) structure of the amorphous-Si (a-Si) TFT device was designed and fabricated. In Fig. 2, the a-Si TFT were fabricated by depositing ferroelectric ferroelectric thin films gate oxide on bottom gate Pt/Ti/SiO_2/Si substrate. A silicon oxide film, acting as a buffer oxide, was deposited on gate oxide substrate by plasma enhanced chemical vapor deposition (PECVD). A amorphous silicon film, acting as an active channel, was also deposited by PECVD method. Additionally, the source and drain regions were doped phosphorous by an ion implantation method. A aluminum films was deposited as the source and drain electrodes.

Finally, the a-Si TFT was heat treated for 1h in N_2 ambient for the purpose of alloying. The a-Si TFT with the dimensions of 40 μm in width and 8 μm in length were designed and fabricated and the I_D-V_G transfer characteristics of 1TC FeRAM devices were measured. The operation characteristic of 1TC structure for TFT devices was similar to SONOS structure of non-volatile flash memory device.

2.1 ABO_3 and $BLSF_s$ structure material

The (ABO_3) pervoskite and bismuth layer structured ferroelectrics (BLSFs) were excellent candidate materials for ferroelectric random access memories (FeRAMs) such as in smart cards and portable electric devices utilizing their low electric consumption, nonvolatility, high speed readout. The ABO_3 structure materials for ferroelectric oxide exhibit high remnant polarization and low coercive filed. Such as Pb(Zr,Ti)O_3 (PZT), $Sr_2Bi_2Ta_2O_9$ (SBT), $SrTiO_3$ (ST), Ba(Zr,Ti)O_3 (BZ1T9), and (Ba,Sr)TiO_3 (BST) were widely studied and discussed for large storage capacity FeRAM devices. The (Ba,Sr)TiO_3 and Ba(Ti,Zr)O_3 ferroelectric materials were also expected to substitute the PZT or SBT memory materials and improve the environmental pollution because of their low pollution problem [9-15]. In addition, the

high dielectric constant and low leakage current density of zirconium and strontium-doped $BaTiO_3$ thin films were applied for the further application in the high density dynamic random access memory (DRAM) [16-20].

2.1.1 ABO3 pervoskite structure material system

For ABO_3 pervoskite structure such as, $BaTiO_3$ and BZ1T9, the excellent electrical and ferroelectric properties were obtained and found. For SOP concept, the ferroelectric BZ1T9 thin film on ITO substrate were investigated and discussed. For crystallization and grain grow of ferroelectric thin films, the crystal orientation and preferred phase of different substrates were important factors for ferroelectric thin films of MIM structures. The XRD patterns of BZ1T9 thin films with 40% oxygen concentration on $Pt/Ti/SiO_2/Si$ substrates from our previous study were shown in Fig. 3 [21-22]. The (111) and (011) peaks of the BZ1T9 thin films on $Pt/Ti/SiO_2/Si$ substrates were compared with those on ITO substrates. The strongest and sharpest peak was observed along the Pt(111) crystal plane. This suggests that the BZ1T9 films grew epitaxially with the Pt(111) bottom electrode. However, the (111) peaks of BZ1T9 thin films were not observed for (400) and (440) ITO substrates. Therefore, we determined that the crystallinity and deposition rate of BZ1T9 thin films on ITO substrates differed from those in these study [21-24].

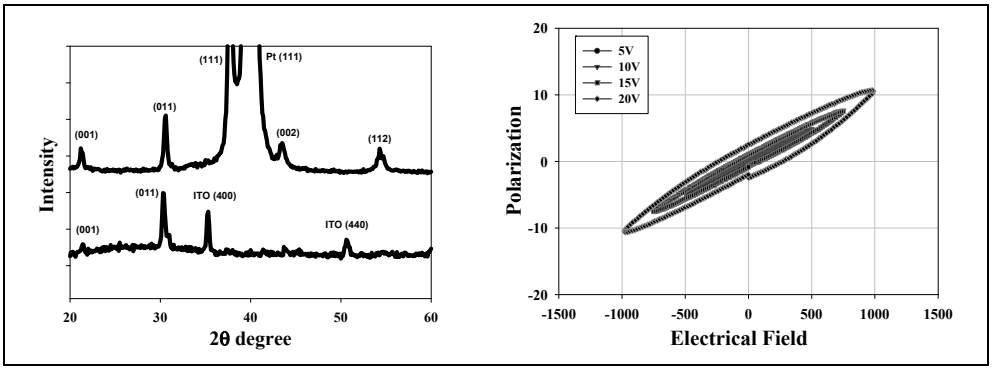

Fig. 3. (a) XRD patterns of as-deposited thin films on the ITO/glass and Pt substrates, and (b) P-E curves of thin films.

The polarization versus applied electrical field (P-E) curves of as-deposited BZ1T9 thin films were shown in Fig. 3(a). As the applied voltage increases, the remanent polarization of thin films increases from 0.5 to 2.5 $\mu C/cm^2$. In addition, the $2P_r$ and coercive field calculated and were about 5 $\mu C/cm^2$ and 250 kV/cm, respectively. According to our previous study, the BZ1T9 thin film deposited at high temperature exhibited high dielectric constant and high leakage current density because of its polycrystalline structure [21].

2.1.2 Bismuth layer ferroelectric structure material system

Bismuth titanate system based materials were an important role for FeRAMs applications. The bismuth titanate system were given in a general formula of bismuth layer structure ferroelectric, $(Bi_2O_2)^{2+}(A_{n-1}B_nO_{3n+1})^{2-}$ (A=Bi, B=Ti). The high leakage current, high dielectric loss

and domain pinning of bismuth titanate system based materials were caused by defects, bismuth vacancies and oxygen vacancies. These defects and oxygen vacancies were attributed from the volatilization of Bi_2O_3 of bismuth contents at elevated temperature [25-27].

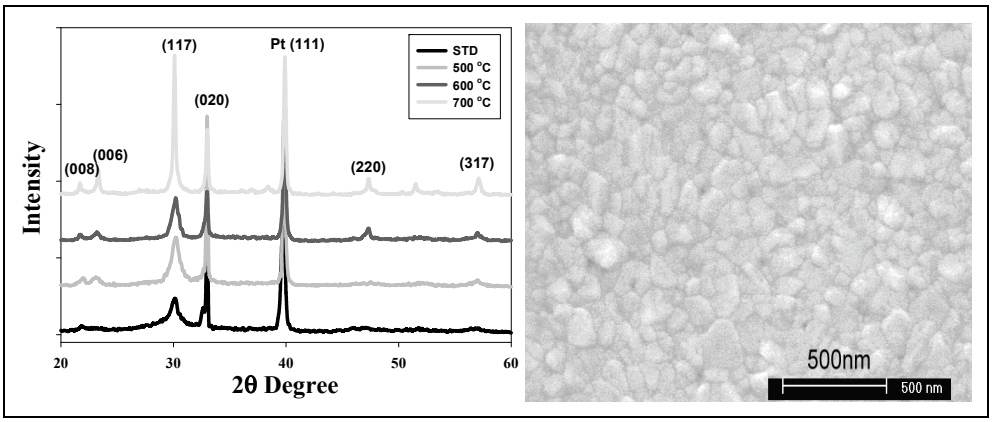

Fig. 4. (a) XRD patterns of as-deposited $Bi_4Ti_3O_{12}$ thin films, and (b)The SEM morphology of as-deposited $Bi_4Ti_3O_{12}$ films.

The XRD patterns of as-deposited $Bi_4Ti_3O_{12}$ thin films and ferroelectric thin films under 500~700°C rapid thermal annealing (RTA) process were compared in Fig. 4. From the results obtained, the (002) and (117) peaks of as-deposited $Bi_4Ti_3O_{12}$ thin film under the optimal sputtering parameters were found. The strong intensity of XRD peaks of $Bi_4Ti_3O_{12}$ thin film under the 700°C RTA post-treatment were be found. They were (008), (006), (020) and (117) peaks, respectively. Compared the XRD patterns shown in Fig. 4, the crystalline intensity of (111) plane has no apparent increase as the as-deposited process is used and has apparent increase as the RTA-treated process was used. And a smaller full width at half maximum value (FWHM) is revealed in the RTA-treated $Bi_4Ti_3O_{12}$ thin films under the 700°C post-treatment. This result suggests that crystal structure of $Bi_4Ti_3O_{12}$ thin films were improved in RTA-treated process.

The surface morphology observations of as-deposited $Bi_4Ti_3O_{12}$ thin films under the 700°C RTA processes were shown in Fig. 4. For the as-deposited $Bi_4Ti_3O_{12}$ thin films, the morphology reveals a smooth surface and the grain growth were not observed. The grain size and boundary of $Bi_4Ti_3O_{12}$ thin films increased while the annealing temperature increased to 700°C. In RTA annealed $Bi_4Ti_3O_{12}$ thin films, the maximum grain size were about 200 nm and the average grain size is 100 nm. As shown in Fig. 4, the thickness of annealed $Bi_4Ti_3O_{12}$ thin films were calculated and found from the SEM cross-section images. The thickness of the deposited $Bi_4Ti_3O_{12}$ thin films is about 800 nm and the deposited rate of $Bi_4Ti_3O_{12}$ thin films is about 14 nm/mim.

2.1.3 The influence of doping effect on the electrical properties of ferroelectric films

In the past, we found that using V_2O_5 as the addition or substitution would improve the dielectric characteristics of $SrBi_2Ta_2O_9$ ceramics [28]. Vanadium doped $Bi_4Ti_3O_{12}$ thin films were also found to have very large remanent polarization (2Pr) and the coercive field (Ec).

But the leakage current density, the memory window and the changing ratio of memory window of vanadium doped $Bi_4Ti_3O_{12}$ thin films measured using the MFIS structure were not developed before [29-31].

Figure 5(a) shows ferroelectric hysteresis loops of $Bi_4Ti_3O_{12}$ and as-deposited BTV thin film capacitors measured with a ferroelectric tester (Radiant Technologies RT66A). The as-deposited BTV thin films clearly show ferroelectricity characteristics. The remanent polarization and coercive field were 23 μC/cm² and 450 kV/cm. To compare the vanadium doped and undoped $Bi_4Ti_3O_{12}$ thin films, the remanent polarization (2Pr) were increased form 16μC/cm² for undoped $Bi_4Ti_3O_{12}$ thin films to 23 μC/cm² for vanadium doped. However, the coercive field of as-deposited BTV thin films would be increased to 450 kV/cm. These results indicated that the substitution of vanadium was effective for the appearance of ferroelectricity at 550 °C. The 2Pr value and the Ec value were larger than those reported in Refs. [9-10], and the 2Pr value was smaller and the Ec value was larger than those reported in [31]. Based on above results, it was found that the simultaneous substitutions for B-site are effective to derive enough ferroelectricity by accelerating the domain nucleation and pinning relaxation caused by B-site substitution [32-35].

Figure 5(b) shows the C-V curves of as-deposited vanadium doped BTV and un-doped BIT thin films. The applied voltages, which are first changed from -20 to 20 V and then returned to -20 V, are used to measure the capacitance voltage characteristics (C-V) of the MFIS structures. For the vanadium doped thin films, the memory window of MFIS structure increased from 5 to 15 V, and the threshold voltage decreased from 7 to 3 V. This result demonstrated that the lower threshold voltage and decreased oxygen vacancy in undoped BIT thin films were improved from the C-V curves measured.

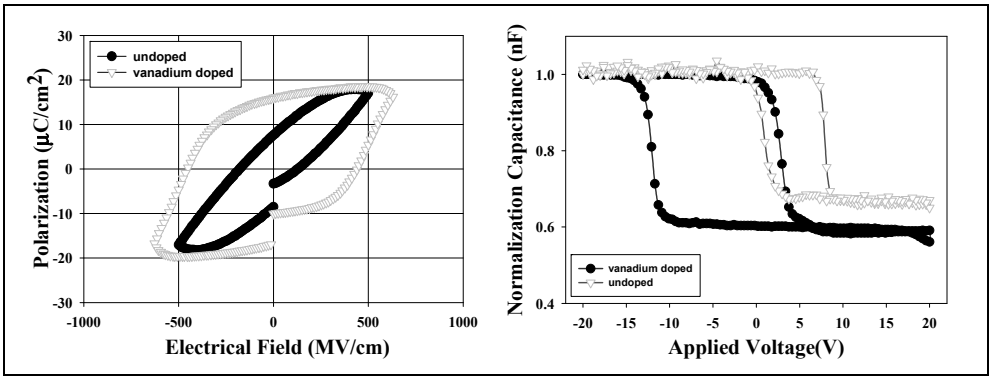

Fig. 5. (a) The P-E characteristics of vanadium doped and undoped thin films, and (b) The normalization C-V curves of vanadium doped and undoped thin films.

According to pervious study, the $Bi_4Ti_3O_{12}$ materials exhibit high leakage current and domain pinning properties because of the defects such as bismuth and oxygen vacancies. The BTV thin film was prepared by substituting a bismuth ion with a lanthanum ion at A-site substitution, and the fatigue endurance characteristics was improved [36]. In addition, the B-site substitution by high-valent cation was mainly the compensation for the defects. These defects caused by the fatigue phenomenon and strong domain pinning [37-40].

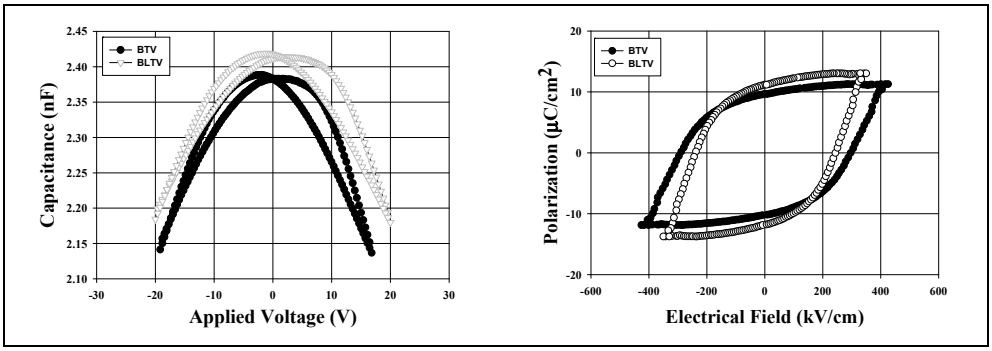

Fig. 6. (a) The C-V characteristics of as-deposited BTV and BLTV thin films, and (b) The P-E characteristics of as-deposited BTV and BLTV thin films.

Figure 6(a) shows the change in the C-V curves of the BTV and BLTV thin films in MFM structure measured at 100 kHz. The applied voltages, which were first changed from -20 to 20 V and then returned to -20 V, were used to measure the capacitance voltage characteristics (C-V). The BLTV thin films exhibited high capacitance than those of BTV thin films. We found that the capacitances of the lanthanum-doped BTV thin films were increased.

Figure 6(b) shows the P-E curves of the different ferroelectric thin films under applied voltage of 18V from the Sawyer–Tower circuits. The remanent polarization of non-doped, vanadium-doped, and lanthanum-doped ferroelectric thin films linearly was increased from 5, 10 to 11 μC/cm², respectively. The coercive filed of non-doped, vanadium-doped, and lanthanum-doped ferroelectric thin films were about 300, 300, and 250 kV/cm, respectively. The ferroelectric properties of lanthanum-doped and vanadium-doped BIT thin films were improved and found.

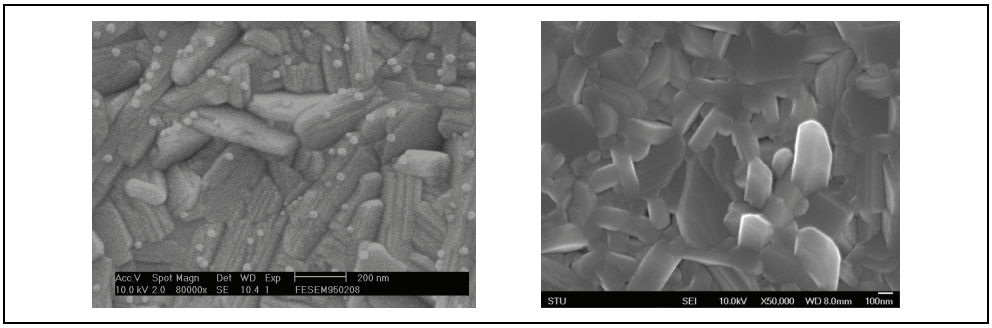

Fig. 7. The surface morphology of as-deposited BTV and BLTV thin films.

In Fig. 7, rod-like and circular-board grains were observed with scanning electron microscopy (SEM) for as-deposited BTV films. The small grain was gold element in preparation for the SEM sample. However, the BLTV thin films exhibited a great quantity rod-like grain structure in Fig. 7. The rod-like grain size of BLTV thin films was larger than those of BTV. We induced that the bismuth vacancies of BTV thin films compensate for lanthanum addition and micro-structure were improved in BLTV thin films.

2.2 Improved properties for ferroelectric films using post-treatment technology

The electrical and physical characteristics were affected by defect and oxygen vacancy of grain boundary in various oxide materials for applications in electrical integrated circuits. The defects and oxygen vacancies in conventional oxide films were usually filled and compensated by oxygen gas using different deposition methods in the semiconductor manufacturing process. The crystal structure of the various oxide films was improved by the high deposition temperature. However, the oxygen elements in grain boundary of the thin films were broken and lost above the deposition temperatures of 550°C [41–47]. To improve the properties of various oxide materials under the post-treatment process, the conventional temperature annealing (CTA) and rapid thermal annealing (RTA) processing were sometimes essential and indispensable technology for crystallization and quality of thin films [48-52].

2.2.1 CFA and RTA post-treatment technology

Ferroelectric thin films prepared by rapid temperature annealing (RTA) and conventional temperature annealing (CFA) processing were reported extensively. Many studies had been reported that rapid temperature annealing method was successfully to increase the electrical and physical properties [53-56]. In addition, grain size, electrical properties and surface roughness are greatly affected by annealing temperature under conventional furnace annealing.

To study the characteristics of thin films of perovskite oxide BZ1T9, deposited on ITO glass substrate using the different RTA annealing temperatures were found. In which, the characteristics of the Al/BZ1T9/ITO glass (MFM) structures, were reported and the relationship between the electrical properties and different annealing temperature of MFM structure was investigated. In addition, preferred orientation, crystal phase and dielectric properties of BZ1T9 thin films by different annealing temperatures were discussion and evaluated.

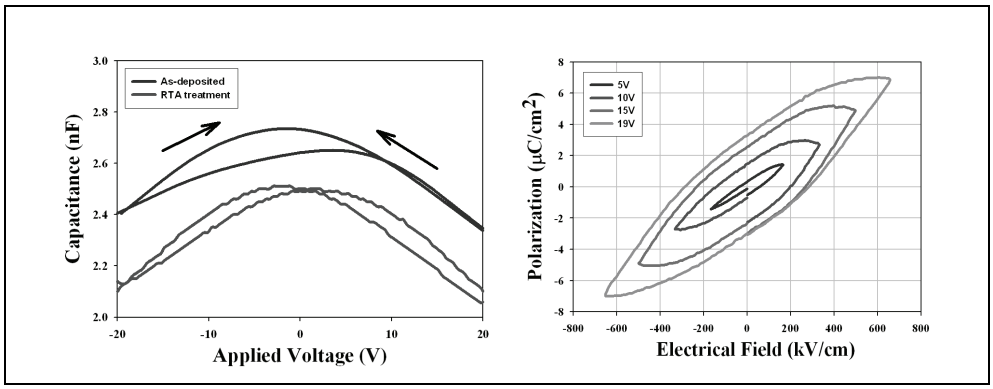

Fig. 8. (a) The C-V characteristics of as-deposited and RTA-treated thin films, and (b) The P-E characteristics of RTA-treated thin films.

Figure 8(a) shows the C-V curves of as-deposited and annealed BZ1T9 films when applied voltage of ±20V. From the experiments obtained, the capacitance of RTA annealed BZ1T9 films increased while the temperature increased to 650°C. Besides, the maximum dielectric

constant of RTA annealed BZ1T9 films were found. In addition, the larger grain size of annealed BZ1T9 films were attributed to this reason.
The leakage current density versus applied electrical field (J-E) curves of as-deposited BZ1T9 films under 650°C RTA process were also found. The leakage current densities of as-deposited BZ1T9 films using RTA process were about 2×10^{-6} A/cm^2 under the electrical field of 0.5 MV/cm. It showed that the leakage current density of annealed-BZ1T9 films was larger than those of as-deposited BZ1T9.
The P-E curves of as-deposited BZ1T9 thin films at a frequency of 100 kHz was shown in Fig. 8(b). As the applied voltage increases, the remanent polarization of thin films increases. In addition, the $2P_r$ and coercive field are also calculated and were about 6 μC/cm^2 and 250 kV/cm, respectively. According to our previous study, the BZ1T9 thin film deposited at a higher temperature exhibits a higher dielectric constant and a higher leakage current density because of its polycrystalline structure [57].

2.2.2 Oxygen plasma post-treatment technology

The high-temperature process for integrated fabrication on electronic devices was a serious problem. The gas-like and excellent properties of the oxygen plasma process were attracted considerable research in efficiently transporting oxygen atom and nodamaging diffusion into the microstructures of oxide materials at a low-temperature treatment. Decreased and passivated the traps and defects of oxide materials were the most advantages.
Figure 9(a) shows the leakage current density versus electrical filed (J-E) curves of as-deposited BSTZ thin films treated as a function of oxygen plasma treatment times. The leakage current density of BSTZ thin films was decreased as oxygen plasma treatment times increased. The leakage current density of treated thin films was lower than those of as-deposited thin films. We also found that the leakage current density of the BSTZ thin films for 3 minutes plasma treatment time were similar to those for 6-9 minutes plasma treatment time. To discuss the defects and oxygen vacancies effect, the leakage current versus electrical field curves were fitted to the Schottky emission and Poole-Frankel transport models [58–60]. The fitting curve was straight line, and the J–E curves of as-deposited thin films after oxygen plasma treatment obey the Schottky emission model in fig. 2. From the experimental results, the low leakage current density of plasma treated thin films was attributed to less oxygen defects and vacancies.
Figure 8(b) shows the capacitances-voltage (C-V) curves of non-treatment and oxygen plasma treatment BSTZ thin films. The capacitance of thin films was increased while the oxygen treatment time increased. The capacitance of thin films was increased. As the results, the improvement of capacitance of BSTZ thin films were attributed to the oxygen ion vacancy compensated.
In addition, we found that the wide-scan XPS spectrum of the as-deposited thin film for oxygen plasma treatment in the binding energy range from 100 to 1keV. From the XPS spectrum, it revealed that the thin films contained Ba 3d, Sr 3d, Ti 2p, Zr 3d, and O 1s elements. After oxygen plasma treated, the LBE and HBE were increased to 533.6 and 535.8 eV. These results induced that the oxygen plasma operatively react with the dangling bonds of thin films and form the stronger O 1s bonding. The O 1s binding energy of the BSTZ thin film after oxygen plasma treatment was increased.

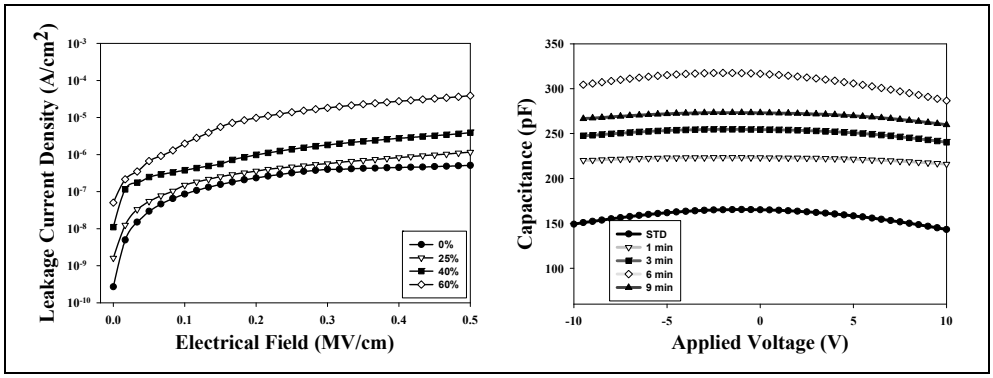

Fig. 9. (a) The J-E characteristics of as-deposited and plasma-treated BSTZ thin films, and (b) The C-V characteristics of as-deposited and plasma-treated BSTZ thin films.

For other ferroelectric thin film, the leakage current density versus applied voltage (J-E) curves of the BZ1T9 thin films was shown in Fig. 5. At an electric field of 0.25 MV/cm, the oxygen-plasma-treated films exhibit a leakage current density two orders of magnitude lower than those of the non-oxygen-plasma-treated ones. As mentioned above, the oxygen plasma treatment decreases the oxygen vacancies and the leakage current density.The current-field curves were fit to Schottky emission and Poole-Frankel transport models to determine whether the observed decrease in leakage current of the oxygen plasma treated films [58-60]. Smyth et al. reported that oxygen escapes during thermal process, and the oxygen vacancies are subsequently generated according to O_o <-> V_o^{++} + 2e$^-$ + 1/2 O_2, that the O_o, V_o^{++}, and e$^-$ denote the oxygen ion at its normal site, oxygen vacancy, and electron, respectively. For that, a lot of oxygen vacancies will exist after 9 min the oxygen plasma treatment.

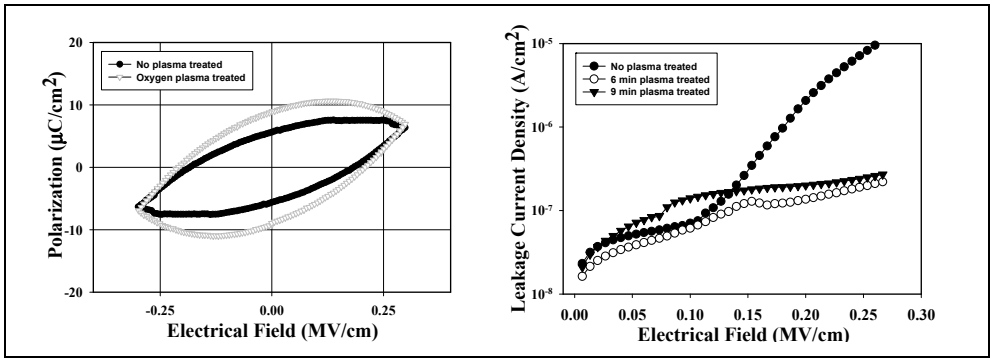

Fig. 10. (a) The P-E characteristics of as-deposited and plasma-treated BZ1T9 thin films, and (b) The J-E characteristics of as-deposited and plasma-treated BZ1T9 thin films.

Figure 10(a) shows the P-E curves of the BZ1T9 films observed at a frequency of 100 kHz under an applied electrical field of 0–0.28 MV/cm from the Sawyer-Tower circuits. After oxygen plasma treatment, the coercive field does not appear to change; however, the remnant polarization appears to increase from 6 to 9 μC/cm2. As shown in Fig. 10(b), we

observed that the saturation polarization decreases slightly when an electrical field of 280 kV/cm was applied. This effect can be caused by the high leakage current density under stronger electrical fields.

2.2.3 Supercritical carbon dioxide fluid technology

To discuses and investigate the electrical, physical, and ferroelectric properties of as-deposited thin films, the supercritical carbon dioxide fluid (SCF) process were used by a low temperature treatment. The ferroelectric thin films were post-treated by SCF process which mixed with propyl alcohol and pure H_2O. After SCF process treatment, the remnant and saturation polarization increased in hysteresis curves, and the passivation of oxygen vacancy and defect in leakage current density curves were found. Besides, the qualities of as-deposited ferroelectric thin films using SCF process treatment were carried out XPS, C-V, and J-E results.

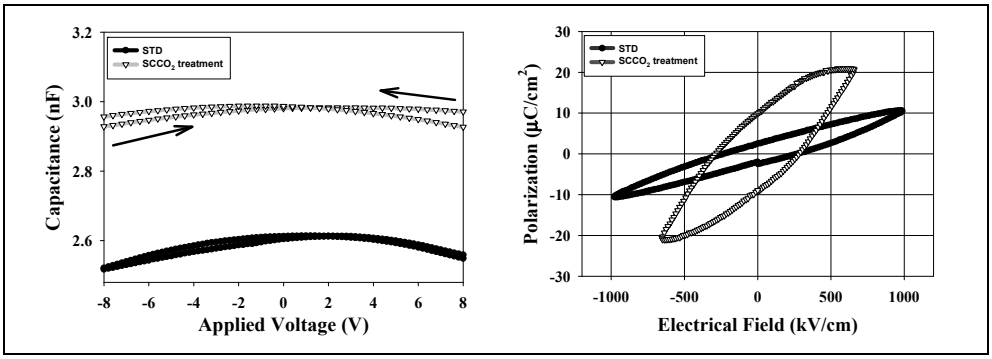

Fig. 11. (a) The C-E characteristics of as-deposited and $SCCO_2$-treated BZ1T9 thin films, and (b) The J-E characteristics of as-deposited and $SCCO_2$-treated BZ1T9 thin films.

Figure 11(a) compares the change in the capacitance versus the applied voltage (C-V) for the non-treatment and $SCCO_2$ fluid treatment BZ1T9 thin films. The applied bias voltage ranges from -20 to 20 V. The capacitances of the BZ1T9 thin films appear to increase due to the $SCCO_2$ fluid treatment. The capacitances increase from 2.65 to 2.95 nF were found after the post-treatment. As suggested by the XPS analysis result, the improvement in the capacitance of the BZ1T9 thin films were attributed to the compensation of the oxygen vacancy of the ABO_3 phase in the BZ1T9 thin films.

Figure 11(b) shows the P-E curves of the thin films observed at a frequency of 500 kHz under a 20V applied voltage from the Sawyer-Tower circuits. After $SCCO_2$ fluid treatment, the 2Pr value and coercive filed of BZ1T9 thin films for MIM structure were about 20 $\mu C/cm^2$ and 250kV/cm, respectively. We found that remnant polarization were improved and increased from 3 to 10 $\mu C/cm^2$.

Figure 12(a) shows the wide-scan XPS spectrum of the BZ1T9 thin film in the binding energy range from 200 to 900 eV. From the spectrum it is clear that the BZ1T9 film contains Ba, Zr, Ti, and O elements near its surface, and no other impurity element was detected in the spectrum up to 900 eV. Quantitative XPS analysis result not only provides the chemical composition near the sample surface, but also gives the formation on the chemical bonding. From the spectrum of the chemical bonding observed, the compounds of the surface for BZ1T9 thin films would be determined. In addition, the narrow-scan XPS spectra of O 1s peaks for the BZ1T9 thin film were shown in Fig. 12(b).

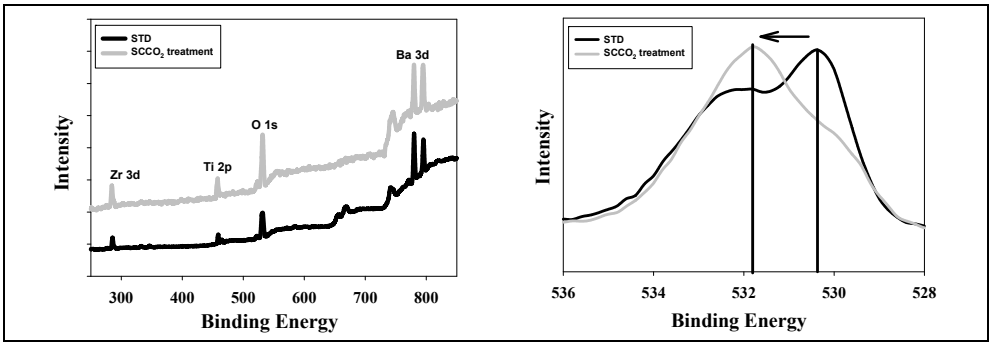

Fig. 12. (a)Wide-scan XPS spectrum and (b) O 1s energy levels of ferroelectric thin film after $SCCO_2$ fluid treatment.

To infer the variation in chemical bonding of BZ1T9 thin films during processing with $SCCO_2$ fluid treatment, a doublet structure was observed in the XPS spectrum of O 1s peak were found. Its component peak in the spectrum was fitted to a Guassian type distribution with lower binding energy (LBE) and higher binding energy (HBE) peaks at 529.62 eV and 531.68 eV, respectively. The LBE peak was due to the oxide and the HBE peak was due to the hydroxide/absorbed oxygen. These results induced that indicating that the H_2O molecules indeed can operatively react with the thin films dangling bonds (or traps) and form the stronger O 1s bonding.

2.3 Fabrication ferroelectric random access memory device on bottom-gated amorphous silicon thin-film transistors

Recently, the ferroelectric BZ1T9 composition was used in a one-transistor-capacitor (1TC) structure of the amorphous-Si TFT device to replace the gate oxide of random access memory devices. For that, a bottom-gate amorphous thin-film transistor, as shown in Fig. 13, was fabricated and the characteristics of the fabricated devices were developed.

The counter clockwise current hysteresis and memory window of n-channel thin-film transistor property were observed, and that were be used to indicate the switching of ferroelectric polarization of BZ1T9 thin films. Additionally, the ferroelectric random access memory device using bottom-gate amorphous silicon thin-film transistor with channel width=40 μm and channel length=8 μm has been successfully fabricated and the I_D-V_G transfer characteristics were also investigated.

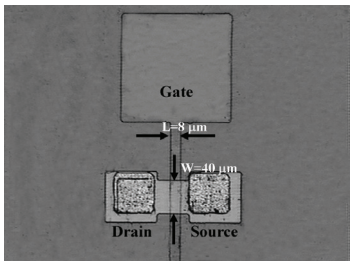

Fig. 13. The top view of the 1TC FeRAM device fabricated with BZ1T9 as the bottom-gate oxide.

After the optimum characteristics of BZ1T9 thin films were deposited, then the BZ1T9 thin films obtained at the optimum parameters were used to fabricate the one-transistor-capacitor (1TC) structure of the amorphous-Si TFT device, and the top view of the fabricated 1TC FeRAM device with BZ1T9 gate oxide was shown. The measured transfer characteristics of drain current and gate voltage (I_D-V_G) of the fabricated ferroelectric gate oxide 1TC FeRAM device were shown in Fig. 14. The a-Si TFT device using BZ1T9 gate oxide measured from the -5 to 20 V and then from 20 return to -5 V at drain voltage from 0.1 to 5V.

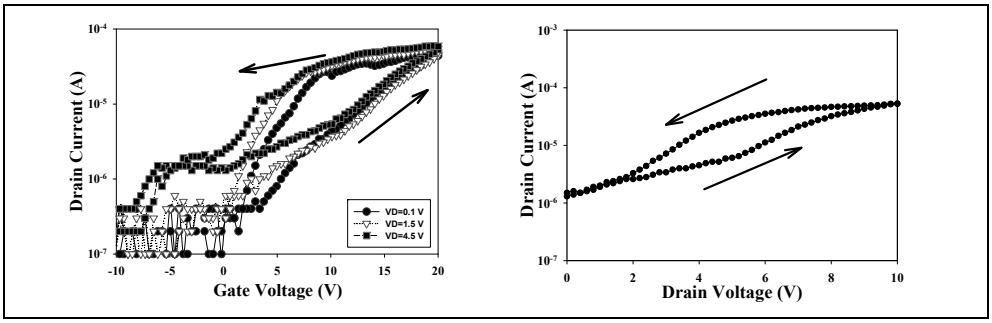

Fig. 14. I_D-V_G transfer characteristics of the fabricated 1TC FeRAM devices.

The counterclockwise current hysteresis and memory window of n-channel thin-film transistor property as indicated by arrows were observed, and the I_D-V_G transfer characteristics were used to indicate the switching of ferroelectric polarization of BZ1T9 thin films. From the measured results, the drain current is less than 1×10^{-7}A around V_G=-1V and larger drain current of 4×10^{-5}A as V_G=10V were found. It was interesting to note that the memory windows are 12 and 20V, respectively, when the drain voltages are increased from 0.1 to 5V. As Fig. 14 shows, the threshold voltage and sub-threshold characteristics were obtained, and threshold voltage was about -4V. Besides, the on/off drain current ratio was about the magnification of two orders. The on/off current ratio obtained from the fabricated 1TC FeRAM device in this study was much smaller than that of the most reported bottom-gated TFTs devices by using different ferroelectric materials as gate oxide.

Figure. 14 shows the measured drain current versus drain voltage (I_D–V_D) characteristics of 1TC FeRAM devices with a channel length of 30 μm. The 1TC FeRAM device has properties typical of n-channel transistors and exhibits clear current saturation. In addition, the (I_D–V_D) current window was found at V_G = 10 V. This was because the ferroelectric gate insulator can induce a considerably large charge. As shown in Fig. 14, we obtained an on-current of 5×10^{-5} A for the 1TC FeRAM devices with a channel length of 30 μm.

3. Conclusion

The post-treatment technology, such as CTA, RTA, $SCCO_2$ and oxygen plasma treatment was an effective method to remove the vacancies and defects for as-deposited ferroelectric thin films. The post-treatment technology was developed to take the oxygen molecules to terminate the traps for as-deposited thin films. The improvement effect in the leakage current mechanism of the as-deposited thin film using post-treatment technology was discussed. The capacitance increased for reduction of interface states and passivation of traps in the as-deposited thin films treated by post-treatment technology was observed.

Besides, the one-transistor-capacitor (1TC) structure of ferroelectric random access memory (FeRAM) with the gate oxide of BZ1T9 thin films on the amorphous-Si TFT structure were investigated and fabricated. The on/off drain current ratio was two orders (10^2), and the value was much smaller than those of the most reported bottom-gated TFTs devices by using different ferroelectric materials as gate oxide. From these results in our study, the BZ1T9 thin film for bottom-gate amorphous-Si thin-film transistor was an excellent candidate to fabricate higher storage capacitance ferroelectric random access memory devices.

4. Acknowledgment

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5. References

[1] J. M. Kim, D. S. Yoon, and K. No: J. Mater. Sci. 29 (1994) 6599.
[2] S. Y. Wu: IEEE Trans. Electron Devices 21 (1974) 499.
[3] S. Y. Wu: Ferroelectrics 11 (1976) 379.
[4] H. Buhay, S. Sinharoy, W. H. Kasner, M. H. Francombe, D. R. Lampe, and E. Stepke: Appl. Phys. Lett. 58 (1991) 1470.
[5] P. T. Liu, Y. T. Chou, L. F. Teng, F. H. Li, H. P. Shieh: Appl. Phys. Lett. 98 (2011) 052102.
[6] J. S. Park, T. S. Kim, K. S. Son, W. J. Maeng, H. S. Kim, M. Ryu, and S.g Y. Lee: Appl. Phys. Lett. 98 (2011) 012107.
[7] M. Kimura, T. Kamiya, T. Nakanishi, K. Nomura, and H. Hosono: Appl. Phys. Lett. 96 (2010) 262105.
[8] K. Sugibuchi, Y. Kurogi and N. Endo: J. Appl. Phys., 46 (1975) 2877.
[9] I. G. Ismailzade, V. I. Nesterenko, Sov. Phys. Crystallogr. 12 (1968) 625.
[10] M. Kimura, T. Sawada, A. Ando, Y. Sakabe, Jpn, J. Appl. Phys. 38 (1998) 5557.
[11] J. F. Scott and C. A. Paz de Araujo, Science 246, 1400 (1989).
[12] D. J. Taylor, R. E. Jones, P. Zurcher, P. Chu, Y. T. Lii, B. Jiang, and S. J. Gillespie, Appl. Phys. Lett. 68, 2300 (1996).
[13] J. F. Scott and C. A. Paz de Araujo, Science 246, 1400 (1989).
[14] C. A. Araujo, J. D. Cuchiaro, L. D. McMillian, M. C. Scott, and J. F. Scott, Nature (London) 374, 627 (1995).
[15] B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, J. Lee, and W. Jo, Nature (London) 401, 682 (1999).
[16] C. C. Leu, L. R. Yao, C. P. Hsu, and C. T. Hu, J. Electrochem. Soc., 157, 3, (2010) G85.
[17] K. H. Chen, Y. C. Chen, C. F. Yang, and T. C. Chang, J. Phys. Chem. Solids, vol. 69, (2008) 461.
[18] C. F. Yang, K. H. Chen, Y. C. Chen, and T. C. Chang, IEEE Trans. Ultrason. Ferroelectr. Freq. Control, 54 (2007) 1726.
[19] C. F. Yang, K. H. Chen, Y. C. Chen, and T. C. Chang, Appl. Phys. A, 90 (2008) 329.
[20] K. H. Chen, Y. C. Chen, Z. S. Chen, C. F. Yang, and T. C. Chang, Appl. Phys. A, 89 (2007) 533.
[21] G. Velu, C. Legrand, O. Tharaud, A. Chapoton, D. Remiens, and G. Horowitz, Appl. Phys. Lett. 79 (2001) 659.

[22] K. H. Chen, Y. C. Chen, C. F. Yang, and T. C. Chang: J. Phys. Chem. Solids 69 (2007) 461.
[23] K. H. Chen, C. F. Yang, C. H. Chang, Y. J. Lin : J. Jap. Appl. Phys., 48 (2009) 091401.
[24] J. Miao, J. Yuan, H. Wu, S. B. Yang, B. Xu, L. X. Cao, and B. R. Zhao, Appl. Phys. Lett. 90 (2001) 022903.
[25]C. F. Yang, K. H. Chen, Y. C. Chen, and T. C. Chang: Appl. Phys. A 90 (2008) 329.
[26] T. Kijima and H. Matsunaga, Jpn. J. Appl. Phys. 38, (1999) 2281.
[27] T. Watanabe, H. Funakubo, M. Osada, Y. Noguchi and M. Miyayama, Appl. Phys. Lett. 80, No.1 (2002).
[28] S. S. Kim, T. K. Song, J. K. Kim and J. Kim, J. Appl. Phys. 92, No.4 (2002)
[29] Y. Noguchi and M. Miyayama, Appl. Phys. Lett. 78, No.13 (2001).
[30] E. K. Choi, S. S. Kim, J. K. Kim, J. C. Bae, W. J. Kim, Y. I. Lee, T. K. Song, Jpn. J. Appl. Phys,Part 1. 43 (1) (2004) 237.
[31]B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, L. Lee, and W. Joe, Nature (London) 401, 682 (1999).
[32] Y. Noguchi, I. Miwa, Y. Goshima, and M. Miyayama, Jpn. J. Appl. Phys., Part 2 39, L1259 (2000).
[33] Y. Noguchi and M. Miyayama, Appl. Phys. Lett. 78, 1903 (2001).
[34] T. Friessnegg, S. Aggarwal, R. Ramesh, B. Nielsen, E. H. Poindexter, and D. J. Keeble, Appl. Phys. Lett. 77, 127 (2000).
[35] W. Takayuki, F. Hiroshi, O. Minoru, N. Yuji, M. Masaru, Appl. Phys. Lett. 80, (2002) 100.
[36] B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, L. Lee, and W. Joe, Nature (London) 401, (1999) 682.
[37] X. J. Meng, J. H. Ma, J. L. Sun, T. Yu, J. Lin, G. S. Wang, J. H. Chu, Appl. Phys. Lett. 78, (2004) 1089.
[38] B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, L. Lee, and W. Joe, Nature (London) 401, (1999) 682.
[39] Y. Noguchi, I. Miwa, Y. Gosima, and M. Miyayama, Jpn. J. Appl. Phys., Part 2 39, (2000) L1259.
[40] Y. Noguchi and M. Miyayama, Appl. Phys. Lett. 78 (2001) 1903.
[41] T. Friessnegg, S. Aggarwal, R. Ramesh, B. Nielsen, E. H. Poindexter, Jpn. J. Appl. Phys., Part 1 40 (2001) 5572.
[42] P. Orgiani, R. Ciancio, A. Galdi, S. Amoruso, and L. Maritato, Appl. Phys. Lett. 96 (2010) 032501.
[43] W. Lim, E. A. Douglas, D. P. Norton, S. J. Pearton, F. Ren, Y. W. Heo, S. Y. Son, and J. H. Yuh, Appl. Phys. Lett. 96, (2010) 053510.
[44] D. Y. Wang, S. Li, H. L. W. Chan, and C. L. Choy, Appl. Phys. Lett. 96, (2010) 061905.
[45] C. C. Lin and C. C. Lee, J. Electrochem. Soc., 157, 2, (2010) A230.
[46] K. Tajima, Y. Yamada, S. Bao, M. Okada, and K. Yoshimura, J. Electrochem. Soc., 157, 3, (2010) J92.
[47] N. C. Su, S. J. Wang, and Albert Chin, Electrochem. Solid-State Lett., 13, 1, (2010) H8.
[48] O. Tuna, Y. Selamet, G. Aygun and L. Ozyuzer, J. Phys. D, 43 (2010) 055402.
[49] K. F. Chiu, C. C. Chen, M. H. Chiang, and W. H. Ho, J. Electrochem. Soc., 157, 2, (2010) A130.
[50] C. C. Chen, K. F. Chiu, K. M. Lin, H. C. Lin, C. R. Yang, F. M. Wang, and M. H. Chiang, J. Electrochem. Soc., 157, 3, (2010) A289.
[51] M. Furuta, T. Nakanishi, M. Kimura, T. Hiramatsu, T. Matsuda, H. Furuta, T. Kawaharamura, C. Li, and T. Hirao, Electrochem. Solid-State Lett., 13, 4, (2010) H101.

[52] S. J. Won, S. S. Sang, W. Lee, G. J. Choi, C. S. Hwang, and H. J. Kim, Electrochem. Solid-State Lett., 13, 2, (2010) G13.
[53] C. L. Sun, P. C. Juan, Y. W. Hsu and Y. W. Liu, Thin Solid Films, 518, 24, (2010) 7433.
[54]C. F. Yang, K. H. Chen, Y. C. Chen, and T. C. Chang, Appl. Phys. A, 90, 2, (2008) 329.
[55] A. D. Li, D. Wu, H. Q. Ling, M. Wang, Z. Liu and N. Ming, J. Cryst. Growth, 235 (2002) 394.
[56] V. R. Palkar, S. Chattopadhyay, S. C. Purandare, S. G. Lokhre, R. Pinto and M. S. Multani, Mater. Lett.33 (1997) 1.
[57] J. Li, L. Zhang, X. Yao and J. Wang, Ceram. Int., 30 (2004) 1509.
[58] M. L. Calzada, A. Gonzalez, R. Jimenez, C. Alemany and J. Mendiola, J. Euro. Ceram. Soc. 21 (2001) 1517.
[59] Y. Wang, L. Li, J. Qi and Z. Gui, Ceram. Int. 28, 6 (2002) 657.
[60] K. H. Chen, Y. C. Chen, C. F. Yang, and T. C. Chang: J. Phys. Chem. Solids 69 (2007) 461.
[61] S. Fleischer, P. T. Lai, and Y. C. Cheng, J. Appl. Phys. 73 (1994) 8353.
[62] T. Mihara and H. Watanabe, Part I, Jpn. J. Appl. Phys. 34 (1995) 5664.
[63] Y. B. Lin and J. Y. Lee, J. Appl. Phys. 87 (2000) 1841.
[64] T. A. Rost, H. Lin and T. A. Rabson, Appl. Phys. Lett., 59 (1991) 3654.
[65] M. Yoshimoto, M. Anami, H. Shinohara, T. Yoshihara, H. Takagi, S. Nagao, S. Kayano and T.Nakano: IEEE Trans., Solid State Circuits, 18 (5) (1983) 479.
[66] T. Matsuda, K. Miyoshi, R. Yamaguchi, S. Moriya and T. Hosoya, K. Harada: IEEE Trans., Solid State Circuits, 20 (1) (1985) 88.
[67] J. Welser, S. Tiwari, S. Rishton, K. Lee and Y. Lee: IEEE Trans., Electron Device Lett., 18 (6)(1997) 278.
[68] N. Young, G. Harkin, R. Bunn, D. McCulloch and I. French: IEEE Trans., Electron Device,43 (11) (1991) 1930.
[69] S. Y. Wu: IEEE Trans., Electron Devices, (1974) 499.
[70] S. Y. Wu: Ferroelectr., 11 (1976) 379.
[71] H. Buhay, S. Sinharoy, W. H. Kasner, M. H. Francombe, D. R. Lampe and E. Stepke, Appl. Phys. Lett., 58 (1991) 1470.
[72] K. Sugibuchi, Y. Kurogi and N. Endo: J. Appl. Phys., 46 (1975) 2877.
[73] T. A. Rost, H. Lin, T. A. Rabson, R. C. Baumann and D. C. Callahan, IEEE Trans. Ultrason. Ferroelectr. Freq. Control, 38 (1991).
[74] S. R. Shannigrahi and H. M. Jang, Appl. Phys. Lett., 79 (2001)1051.
[75] S. K. Hong, C. W. Suh, C. G. Lee, S. W. Lee, E. Y. Hang and N. S. Kang: Appl. Phys. Lett., 77 (2000) 76.
[76] S. B. Xiong and S. Sakai: Appl. Phys. Lett., 75 (1999) 1613.
[77] J. S. Kim and S. G. Yoon: J. Vac. Soc. Technol., B 18 (1) (2000) 216.
[78] T. B. Wu, C. M. Wu and M. L. Chen: Appl. Phys. Lett., 69 (1996) 2659.
[79] M. She, H. Takeuchi and T. J. King: IEEE Trans., Electron Device Lett., 25 (5) (2003) 309.
[80] Y. K. Lee, J. S. Sim, S. K. Sung, C. J. Lee, T. H. Kim and J. D. Lee: IEEE Trans., Electron Device Lett., 23 (11) (2002) 664.
[81] M. W. J. Prins, K. O. Grosse-Holz, G. Muller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening and R. M. Wolf: Appl. Phys. Lett., 68 (1996) 3650.
[82] T. Miyasako, M. Senoo and E. Tokumitsu: Appl. Phys. Lett., 86 (2005).

9

Ferroelectric Copolymer-Based Plastic Memory Transistos

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1. Introduction

Flexible electronic devices and systems fabricated on bendable, rollable, and stretchable plastic substrate define important application fields of novel paradigm for next-generation "consumer electronics". In these fields, such features as good design, ultra-low cost, and unique functionality would be primarily demanded, which is totally different from the case of conventional Si-based electronics. Recently, many types of interesting approaches have been actively researched and developed. Flexible displays (Gelinck & Leeuw, 2004; Park J. S. et al., 2009), radio-frequency flexible identification tags (Forrest, 2004; Jung M. et al., 2010), flexible and stretchable sensor arrays (Lin K. & Jain, 2009; Someya et al., 2005), flexible electronic circuit systems (Graz & Lacour, 2009; Zschieschang et al, 2010), stretchable lightings (Sekitani et al., 2009a), printable devices (Ishida et al., 2010), and sheet-type communication and power-transmission system (Sekitani et al., 2009b) are the feasible examples. In order to develop the practical systems using these devices, an embeddable nonvolatile memory is strongly required as one of the core devices. The employment of suitable memory device into the systems can effectively reduce their power consumption (Chu et al., 2010; Ueda et al., 2010) as well as enhance their functions by storing the information. Therefore, if the nonvolatile memory devices having features of mechanical flexibility, lower power operation, higher device reliability, and simpler fabrication process at lower temperature would be successfully realized, it would make great impacts on the related fields.

So far, various methodologies using different operating origins and material combinations have been tried to realize the nonvolatile memory functions on the flexible plastic substrates. They can be roughly classified into several types according to the active materials and device structures. Reversible resistance change in organic layer has been exploited for the plastic memory applications, which is operated by reduction-oxidation reaction of the organic layer (Novak et al., 2010), charge-trapping/detrapping within the organic composite (Cho B. et al., 2010) or conductive filament formation between the top and bottom electrodes sandwiching

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the organic films (Ma et al., 2004). The bending characteristics of the resistive-type nonvolatile polymer memory device fabricated on the poly(ethylene terephthalate) were well demonstrated (Ji Y. et al., 2010). In place of organic layers, binary oxide thin-films which can be deposited at low temperature were also employed for the resistance change operation (Lee S. et al., 2009; Seo J. W. et al., 2009). The feasibility for the three-dimensional stacked memory concept was also introduced by implementing one-diode (CuO/InZnO)-one-resistor (NiO) storage node with InGaZnO (IGZO) thin-film transistors (Lee M. J. et al., 2009). Charge-injection has also been utilized for the nonvolatile memory operation, for which specified device structures such as organic bilayers (Ma et al., 2002) or nanoparticle-embedded organic layers (Leong W. L. et al., 2009) have been proposed. Organic thin-film transistor having a floating-gate for charge storing is one of the most typical memory transistors fabricated on the plastic substrates (Baeg K. J., 2010; Wang W. et al., 2009). On the other hand, the ferroelectric-based field effect transistor (FeFET) have features that remnant polarization of ferroelectric gate insulator can be employed for the nonvolatile memory actions (Kang S. J. et al., 2009a; Lim S. H. et al., 2004). Although each device configuration has pros and cons, the practical memory array embeddable into the flexible electronic systems have not been yet commercialized.

Tracing the nonvolatile memory technologies in Si-based electronics back to 1990s, the FeFET was one of the most promising devices replacing the conventional flash memory facing physical scaling limitations at those times. However, the crosstalk for random accessibility and short data retention time of the FeFET were concluded to be fatal drawbacks for the mass-production, although it successfully claimed the ultimate scalability and nondestructive readout characteristics. Unlike these situations in the Si-based electronics demanding an ultra-high specifications and an aggressive device scaling, the requirements for the nonvolatile memory devices integrated into the large-area electronics including the flexible systems are considerably different. In these fields, low-cost and stable operation would be more important factors than the high performances. From this viewpoint, the ferroelectric field-effect thin-film transistor employing a polymeric ferroelectric material, instead of oxide ferroelectrics, can be a very promising candidate because it can be operated in a very reproducible way with a definitely designable operation principle and be fabricated by a very simple process. In this chapter, we propose the organic/inorganic hybrid-type plastic memory transistor exploiting the ferroelectric field effect with the gate stack structures of ferroelectric copolymer gate insulator and oxide semiconducting active channel. Our device concept and features of ferroelectric copolymer-based memory transistor will be proposed in Section 2. The device characteristics and nonvolatile memory behaviors of the proposed plastic memory transistors are demonstrated and the remaining technical issues to solve for future practical applications are picked up. This approach will provide a special meaning to expand the ferroelectric nature to the next-generation large-area electronics.

2. Flexible ferroelectric memory

As mentioned above, the single-transistor-cell-type memory transistors composed of a ferroelectric gate insulator (GI) have been extensively investigated for the conventional Si electronics so far, in which various oxide ferroelectric materials such as $Pb(Zr,Ti)O_3$ (Shih W. C. et al., 2007; Tokumitsu et al., 1997), $SrBi_2Ta_2O_9$ (Horiuchi et al., 2010; Tokumitsu et al., 1999; Yoon S. M. et al., 1999), $(Bi,La)_4Ti_3O_{12}$ (Aizawa K. et al., 2004; Lee N. Y. et al., 2003),

$PbGeO_3$ (Li T. et al., 2003), $YMnO_3$ (Ito D. et al., 2003), $LiNbO_3$ (Kim K. H., 1998), and $BiFeO_3$ (Lin C. et al., 2009) have been chosen as the ferroelectric GI. However, in realizing the plastic nonvolatile memory array, the use of oxide ferroelectric GI is absolutely unfavorable owing to the high crystallization temperature which is typically higher than 650 °C. The overall process temperature should be suppressed below 200 °C. Although some encouraging reports on the novel transfer technique (Roh J. et al., 2010) and ultra-low temperature process (Li J. et al., 2010) for the oxide ferroelectric thin films have recently been published, to secure the high-quality oxide ferroelectric GI for the memory transistor with low temperature process is still very challenging. From this background, the employment of polymeric ferroelectric thin film can offer an attractive solution to this problem because its crystallization temperature is much lower than those of the oxide ferroelectrics. Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] is the most typical ferroelectric copolymer material (Furukawa T., 1989; Nalwa H. S., 1995). It shows superior properties of a relatively large remnant polarization, a short switching time, and a good thermal stability when it is compared with other organic ferroelectric materials such as odd-nylon, cynopolymer derivatives, polyurea, ferroelectric liquid crystal polymers (Nalwa H. S., 1995). The melting temperature, Curie temperature, and crystallization temperature are changed with the composition of PVDF and TrFE. For the composition of 70/30 mol% for the P(VDF-TrFE), those properties are known as 155 °C, 106 °C, and 129 °C, respectively. The remnant polarization (P_r) and dielectric constant are in the ranges from 8 to 12 $\mu C/cm^2$ and from 12 to 25 , respectively, depending on the composition (Nalwa H. S., 1995). P(VDF-TrFE) thin film can be simply formed by a solution-based spin-coating method and be crystallized at a lower temperature around 140 °C, which is one of the beneficial merits in realizing the memory device on the plastic substrate.

So far, most works on the fabrication and characterization for the nonvolatile memory transistors using the P(VDF-TrFE) have been mainly investigated for realizing the all-organic memory transistors with organic semiconducting channel layers. Various organic active layers such as the evaporated pentacene (Kang S. J. et al., 2008; Nguyen C. A. et al., 2008; Schroeder R. et al., 2004), soluble pentacene (Kang S. J. et al., 2009a;b), and solution-processed polymeric semiconductors (Naber R. C. G. et al., 2005a;b) were chosen and the memory thin-film transistors were demonstrated. Actually, it is the case that the employment of organic channel can be very suitable for low-cost disposable applications with a lower specification. However, the weaknesses of a low field-effect mobility, a unsatisfactory ambient stability, and a difficult device integration with the organic-based transistors seriously restrict the real application of this kind of memory TFT within narrow limits. A powerful alternative for enhancing and stabilizing the device performance is to utilize the oxide semiconductor such as ZnO and IGZO, which is one of the most important features of our proposed plastic memory transistor. The oxide semiconductor-based TFTs present such beneficial features as high field-effect mobility, excellent uniformity, and robust device stability (Hoshino K. et al., 2009; Jeong J. K. et al., 2008; Nomura et al., 2004). As results, the oxide TFTs have attracted huge interest as one of the most promising backplane device technologies for the next-generation liquid-crystal display (LCD) (Osada T. et al., 2010) or organic light-emitting diode display (OLED) (Ohara H. et al., 2010; Park J. S. et al., 2009) with a large size and a high resolution. A transparency of the oxide semiconductor to the visible light can be another benefit of expanding the applications to the transparent electronic devices (Park S. H. et al., 2009). These features can be similarly applied for the ferroelectric-based plastic memory transistors. Because the oxide channels are patterned into only small gate areas on the substrate, a relatively brittle nature of oxide

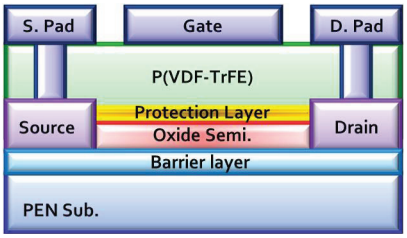

Fig. 1. Typical example of a schematic cross-section diagram for the proposed plastic memory TFT.

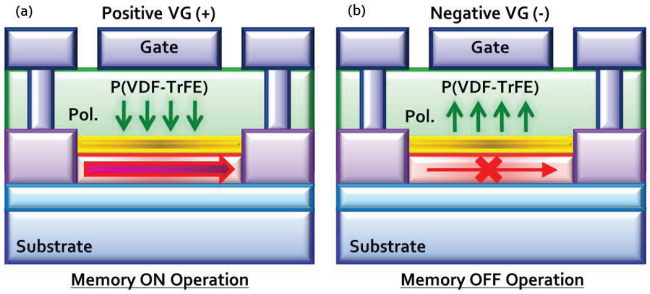

Fig. 2. Schematic views on the operating origin for the nonvolatile memory behaviors of the ferroelectric field-effect-driven memory TFT. When the oxide semiconductor is considered to be n-type, positive and negative programming voltage are initially applied to the gate terminal for (a) *on* and (b) *off* operations, respectively.

thin-film will be no longer a fatal problem for the flexible electronic devices. The use of oxide channel for the plastic memory TFT is also preferable in the viewpoint of integrating the full-scale memory array with memory cells and peripheral driving circuit. Because the oxide TFTs are very suitable devices composing the circuit components, we can design the process using common oxide channels for both the memory and driving TFTs. On the basis of the considerations discussed above, the combination of an organic ferroelectric gate insulator and an oxide semiconducting channel will be the best choice for the high performance nonvolatile memory transistors embeddable into the various electronic systems implemented on the large-area flexible plastic substrate.

Figure 1 shows a typical schematic cross-sectional view of our proposed plastic memory TFT, which was designed to be a top-gate bottom-contact configuration. Because the P(VDF-TrFE) is vulnerable to the plasma-induced deposition process for the oxide channel layer, the bottom-gate configuration is very difficult to be fabricated with an excellent interface between the P(VDF-TrFE) and oxide semiconductor. Furthermore, in order to enhance the device performances, the post-annealing process is sometimes performed at a temperature higher than 200 °C after the deposition of oxide channel. However, the available thermal budget after the formation of P(VDF-TrFE) is restricted to below 150 °C for the bottom gate structure owing to the low melting temperature of the P(VDF-TrFE). The interface controlling layer in the top-gate structure, as shown in the figure, is very desirable to be introduced between the P(VDF-TrFE) and oxide channel layer. In this work, a very thin Al_2O_3 layer deposited by

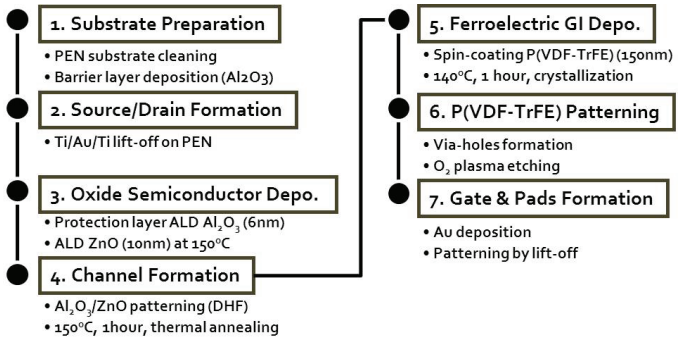

Fig. 3. Flowchart of fabrication procedures for the proposed plastic memory TFT, in which the process steps were designed to use four photomasks. All processes were performed below 150 °C.

atomic-layer deposition (ALD) method was prepared for the device fabrication. This interface controlling layer is very effective for protecting the channel surface during the coating and etching processes of the P(VDF-TrFE) GI layer. Chemical solvents of the P(VDF-TrFE) solution and/or oxygen plasma environment employed for the P(VDF-TrFE) patterning process might degrade the electrical natures of the oxide channel layers. The operating origin for the nonvolatile memory behaviors of the proposed memory TFT can be explained by simple schematics shown in Fig. 2. When the positive gate voltage is applied, the ferroelectric polarization of the P(VDF-TrFE) aligns downward and hence the large drain current flow in the n-type oxide channel layer between the source and drain terminals. Because the aligned polarization remained even after the removal of the gate voltage, the programmed drain current can be detected when the drain is biased. This is the memory *on* state. On the other hand, after the negative gate voltage is applied, the polarization aligns upward, and hence the device doesn't flow the current through the channel. This is the memory *off* state. The programmed data can be nondestructively readout in the shape of drain current, because the read-out signals are so chosen as not to reverse the direction of pre-aligned ferroelectric polarization. In order to guarantee the good memory operations of the proposed memory TFT, it is very important to carefully design and optimize some parameters of thicknesses in the interface controlling and oxide channel layers. The detailed strategies can be referred in our previous investigation (Yoon S. M. et al., 2009a). We previously demonstrated the feasibility of our proposed memory TFTs fabricated on the glass substrate. The excellent device characteristics of the memory TFT using P(VDF-TrFE) GI and IGZO active channel was successfully confirmed, in which a thermal budget for overall process was 250 °C (Yoon S. M. et al., 2010a). The fully-transparent memory TFT using Al-Zn-Sn-O active channel was fabricated to have the transmittance of approximately 90% at a wavelength of 550 nm (Yoon S. M. et al., 2010b). Write and read-out operations of the two-transistor-type memory cell composed of one-memory and one-access oxide TFTs, which was integrated onto the same substrate, were also demonstrated (Yoon S. M. et al., 2010c). In this work, we will focus on the fabrication and characterization of the flexible nonvolatile memory TFT prepared on the plastic substrate.

3. Experimetal details

Poly(ethylene naphthalate) (PEN, Teijin DuPont) was selected as a substrate owing to its low coefficient of thermal expansion, strong chemical resistance, and low-cost for the device fabrication. Firstly, barrier against the out-gassing and surface planarization layer of ALD-grown Al_2O_3 was prepared onto the bare PEN substrate. Ti/Au/Ti film was deposited by electron-beam (e-beam) evaporation and patterned into the source/drain electrodes on the 200-μm-thick PEN by lift-off process. Top and bottom layers of Ti worked as good ohmic contact with oxide channel layer and good adhesion with the substrate, respectively. 10-nm-thick ZnO film was chosen as an oxide semiconducting channel for the plastic memory TFT, which was deposited by plasma-enhanced ALD method at 150 °C using diethylzinc and O_2 plasma as the Zn and oxygen sources, respectively. Then, 6-nm-thick Al_2O_3 interface controlling layer was successively deposited by ALD method at 150 °C using trimethylaluminium and water vapor as the Al and oxygen sources, respectively. After the Al_2O_3 and ZnO were patterned into the channel areas using dilute hydrofluoric acid solution, thermal treatment was performed at 150 °C to enhance the ZnO channel properties. P(VDF-TrFE) layer was formed by spin-coating method using a 2.5 wt% dilute solution of P(VDF-TrFE) (70/30 mol%) in methyl-ethyl-ketone. A solution was spun on the substrate at a spin rate of 2000 rpm and then dried at 70 °C for 5 min on a hot plate. The prepared film was crystallized at 140 °C for 1 h in an air ambient. The film thickness of P(VDF-TrFE) was measured to be approximately 150 nm. Via-holes were formed by O_2 plasma etching of the given areas of P(VDF-TrFE) layer using a dry etching system, in which the lithography processes including the developing and stripping of photoresists coated on the P(VDF-TrFE) layer were so carefully designed as not to make undesirable chemical damage to the P(VDF-TrFE) (Yoon S. M. et al., 2009b). Finally, Au film was deposited by e-beam evaporation and patterned as gate electrode and pads via lift-off process. The process flow and the detailed conditions were summarized in Fig. 3. Figures 4(a) and (b) show a photograph of the process-terminated PEN substrate and a typical photo-image of the substrate under a bending situation, respectively. The size of the test-vehicle processed on the PEN substrate was 2×2 cm^2. The microscopic top view of the memory TFT fabricated on the PEN substrate was shown in Fig. 4(c). All the electrical characteristics including programming and retention behaviors of the fabricated plastic memory TFT were evaluated in a dark box at room temperature using a semiconductor parameter analyzer (Agilent B1500A). The variations in their characteristics under the bending situation with a given curvature radius (R) were measured by setting the configuration, as shown in Fig. 4(d).

4. Device evaluations

4.1 Bending characteristics of ferroelectric P(VDF-TrFE) capacitors

In advance, the basic ferroelectric behaviors were investigated for the P(VDF-TrFE) capacitors which were fabricated with the TFTs on the same substrate. Figure 5(a) and (b) show a schematic cross-sectional diagram and a top-view of optical microscope for the Au/P(VDF-TrFE)/Au capacitors. Patterned P(VDF-TrFE) film was accurately defined between the top and bottom electrodes with the capacitor size of 25×25 μm^2. The polarization-electric field (P-E) characteristics of the ferroelectric capacitor were measured as shown in Fig. 5(c), in which the E was modulated from 0.45 to 1.80 MV/cm. Typical values

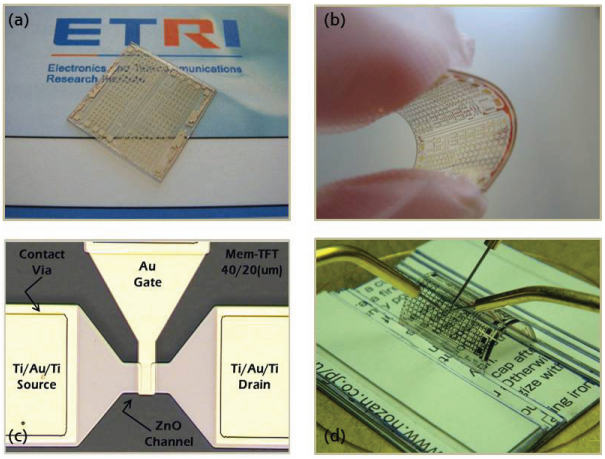

Fig. 4. (a) A Photograph of the PEN substrate on which the test devices were fabricated. (b) A typical photo image of the PEN substrate under a bending situation. The substrate size is 2×2 cm^2. (c) Microscopic top view of the fabricated memory TFT with the structure of Au/P(VDF-TrFE)/Al_2O_3/ZnO/Ti/Au/Ti/Al_2O_3/PEN. The channel width and length are 40 and 20 μm, respectively. (d) A photo image of electrical evaluation for the fabricated device when the PEN substrate was bent with R of 0.65 cm.

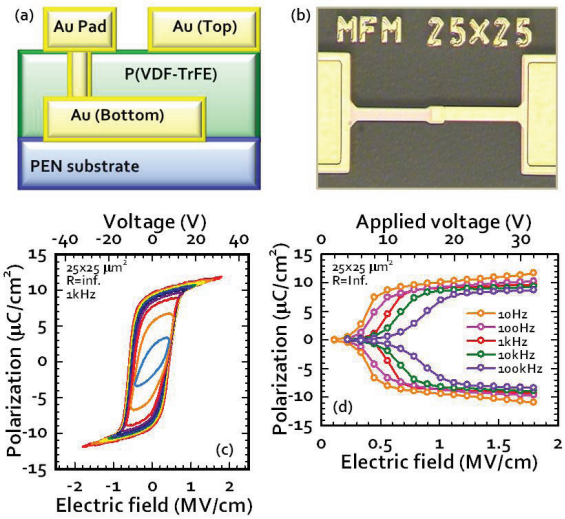

Fig. 5. (a) A Schematic cross-sectional diagram and (b) a microscopic image of the evaluated P(VDF-TrFE) capacitors fabricated on the PEN substrate. The patterned capacitor size was 25×25 μm^2. (c) A typical P-E characteristics of the P(VDF-TrFE) capacitors fabricated on the PEN substrate at the frequency of 1 kHz. (d) Polarization saturation behavior with the increase in the E applied across the capacitor at various signal frequencies from 10 Hz to 100 kHz.

of the remnant polarization (P_r) and coercive field (E_c) were obtained to be approximately 9.1 μC/cm^2 and 522 kV/cm, respectively, at the measuring signal frequency of 1 kHz. The polarization saturation behaviors with the increase of the E applied across the ferroelectric film were also examined at various signal frequencies from 10 Hz to 100 kHz, as shown in Fig. 5(d). The E required to obtain the full saturation in the ferroelectric polarization was observed to decrease with the decrease in signal frequency, which is related to the fact that the memory operations of the proposed plastic memory TFT may be influenced by the duration of programming voltage signals as well as the signal amplitudes (Furukawa T. et al., 2006; 2009; Yoon S. M. et al., 2010d). It can be said that these obtained characteristics were almost similar to those for the P(VDF-TrFE) capacitors fabricated on the Si or glass substrate, even they were prepared on the flexible PEN substrate.

It is very important to investigate the variations in electrical properties of the fabricated capacitors when the substrate was bent with a given curvature radius (R). In these measurements, the R was set to be two values of 0.97 and 0.65 cm, as shown in Figs. 6(a) and (b), respectively, which visually show the bending situations of the substrate. Figures 6(c) and (d) show the P-E ferroelectric hysteresis curves of the same device examined in Fig. 5 when the R's were 0.97 and 0.65 cm, respectively. There was no problem in obtaining the ferroelectric polarization for the P(VDF-TrFE) capacitors even under the bending situations. The detailed variations with the changes in R can be confirmed in Fig. 7(a), in which P-E curves obtained at the same field for the bending situations with different R's were compared. The P_r was varied to approximately 9.6 μC/cm^2 when the R decreased to 0.65cm, which correspond to the increase by 5% compared with the case when R was infinite (∞). However, this small increase in P_r can be explained by the increase in leakage current component for the examined device owing to the repeated evaluations under a high electric field. As a result, it can be suggested that the capacitor did not experience a significantly remarkable variation in the ferroelectric properties. On the other hand, the E_c was measured to be approximately 528 and 588 kV/cm when the R was set to be 0.97 and 0.65 cm, respectively. Although it was observed that there was an approximately 13% increase in E_c when the substrate was bent with R of 0.65 cm, it is likely that this does not originated from the mechanical strain induced by the substrate bending. The detailed effects of the bending R on the polarization saturation behaviors were examined as shown in Figs. 7(c) and (d) at two signal frequencies of 10 Hz and 10 kHz, respectively. It is very useful to introduce a parameter of E_{hp} in order to quantitatively compare the obtained characteristics for the different bending situations. The E_{hp} was defined as the electric field required for securing the half point of full saturation of ferroelectric polarization ($0.5P_r$) at a given signal frequency. For the signal frequency of 10 Hz [Fig. 7(c)], the E_{hp}'s for the various R's of ∞, 0.97, and 0.65 cm were estimated to be approximately 0.38, 0.41, and 0.44 MV/cm, respectively. On the other hand, at the signal frequency of 10 kHz [Fig. 7(d)], the E_{hp}'s were approximately 0.67, 0.72, and 0.81 MV/cm for the same situations. These observations might indicate that the polarization switching at initial phase for the lower electric field was impeded when the P(VDF-TrFE) film was bent, and that the extent of impediment was larger for the cases of larger R and higher signal frequency. However, these kinds of evaluation are sometimes very tricky and controversial. It was also observed that the E_{hp} showed larger values when the substrate was restored to the initial flat status (R=∞) compared with those for the R of 0.65 cm, as shown in Figs. 7(c) and (d). Consequently, it can be concluded that the larger impediment in polarization switching event, which was mainly observed for the larger R, was dominantly affected by the ferroelectric fatigue, even

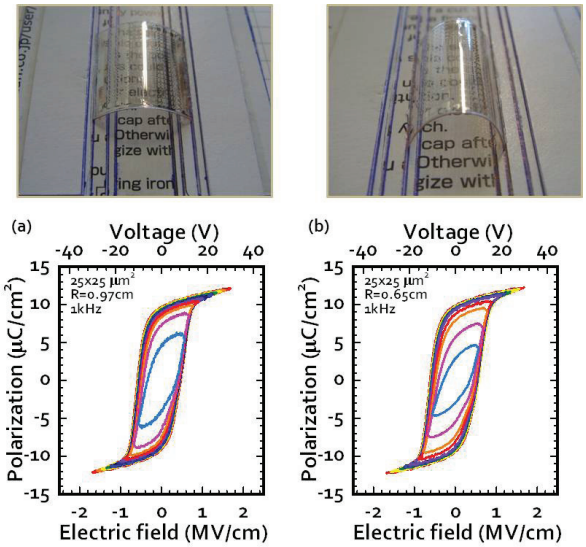

Fig. 6. *P-E* characteristics of the Au/P(VDF-TrFE)/Au capacitors when the substrate was bent with different *R*'s of (a) 0.97 and (b) 0.65 cm. The bending situations of each case are shown in photos. The measurement frequency was set to be 1 kHz.

though some parts of degradation caused by the mechanical strain at the bending situation cannot be completely ruled out. It gives more detailed insights to investigate the bending characteristics of the device with different capacitor size, as shown in Fig. 7(b), because the mechanical strain is differently induced for the capacitors with different size even for the same *R*. According to the obtained characteristics for the P(VDF-TrFE) capacitors with the size of 200×200 μm^2, there was not any marked variation in the behaviors except for the small increase in E_c with the decrease of *R*. It suggests that the polarization saturation behaviors behaved in a very similar way to those discussed above for the 25×25-μm^2-sized capacitor even for the larger capacitor size. We can found from these discussions that the mechanical strain applied to the P(VDF-TrFE) capacitors under the bending situations did not make any critical influence on the ferroelectric properties, which is in a good agreement with the previous reports (Matsumoto A. et al., 2007; Nguyen C. A. et al., 2008). However, the data reproducibility and further investigations should be also performed with smaller *R* to accurately verify the bending effects on the device as future works.

4.2 Memory behaviors of flexible memory TFT

Based on the basic ferroelectric properties of the P(VDF-TrFE) capacitors fabricated on the PEN substrate, the device characteristics of the fabricated memory TFT were extensively investigated. Figure 8(a) shows the drain current-gate voltage (I_D-V_G) transfer characteristics of the plastic memory TFT at the various sweep range in V_G, which were measured with a double sweep mode of forward and reverse directions at V_D of 5.0 V. The gate width (W) and length (L) of the measured device were 40 and 20 μm, respectively. As can be seen in the figure, we could obtain sufficiently good device performances, in which the 8-orders-of

magnitude on/off ratio and the subthreshold swing (SS) of 650 mV/dec were successfully obtained. Counterclockwise hystereses of the transfer curves which originated from the ferroelectric field effect were clearly observed. A 3.4 V-memory window was obtained at the V_G sweep range from -10 to 8 V. Gate leakage currents could be suppressed to be lower than 10^{-11} A, even though the device was fabricated on the plastic substrate using low-temperature processes below 150 °C. It was confirmed that the transfer characteristics did not change between the first and the second sweep in V_G, as shown in Fig. 8(b). This is also an important point considering the fact that the transfer curves of this kind of memory TFT are markedly fluctuated if the fabrication processes are not optimized for the device. Although only twice repetitive measurements of transfer curves cannot guarantee the endurance in device performance, the undesirable variations in device characteristics during the repetitive operations could be easily examined even by performing only two successive sweeps. Therefore, it can be concluded that the proposed plastic memory TFT was well fabricated on the PEN substrate without any critical damages caused by fabrication processes. The bending characteristics were also investigated for the same device, in which two kinds of measurements were performed. The first one is to examine the changes in device behaviors at the situations of substrate bending with a given R, which can be called as "bending durability". The second one is to evaluate the degradation in device performance after the given numbers of repetitive bending operation, which can be called as "bending fatigue endurance". Figure 9(a) shows the bending durability by measuring the transfer characteristics when the substrate was bent with the R of 0.97 cm. As can be seen in the figure, the plastic memory TFT did not experience so marked variations in its device behaviors. The change in memory window at the bending situation was approximately 0.7 V at most. It was also very encouraging that the bending fatigue endurance test with 20,000 cycles did not make any critical degradation in its characteristics, as shown in Fig. 9(b). In this evaluation, bending fatigue was intentionally loaded by using the specially-designed bending machine shown in Figs. 9(c) and (d), in which the R was set to be 2.35 cm. These results indicate that the proposed plastic memory TFT fabricated on the PEN can be utilized under the bending situations for any flexible devices. Although the R could not be reduced to smaller state owing to the substrate size and machine specification in this work, further investigations would be necessary when the device is repeatedly bent for larger number of bending at smaller R. Actually, we have to check the observation that a very small reduction in the memory window was observed as the increase in the number of bending.

Finally, the programming and retention behaviors of the fabricated plastic memory TFT were evaluated, as shown in Fig. 10. These characteristics are very important for actually employing the nonvolatile memory component embedded into the large-area flexible electronic systems. The programming events for the *on* and *off* states were performed by applying the voltage pulses of 6 and -8 V, respectively. The pulse width was varied to 1 s and 100 ms in order to estimate the relationship between the available memory margin and the programming time. Both memory states were detected by measuring the I_D at a read-out V_G of 0 V. The memory window in transfer curve for the memory TFT, which was obtained to be located with centering around 0 V in V_G [Fig. 8], is a very beneficial property, because the read-out and retention operations for the stored information can be carried out at 0 V. For the case of 1 s-programming, the *on/off* ratio was initially obtained to be approximately 6.6×10^5 and it decreased to approximately 130 after a lapse of 15000 s. On the other hand, for the case of 100 ms-programming, the initial *on/off* ratio was only 8.0×10^3 and the memory margin

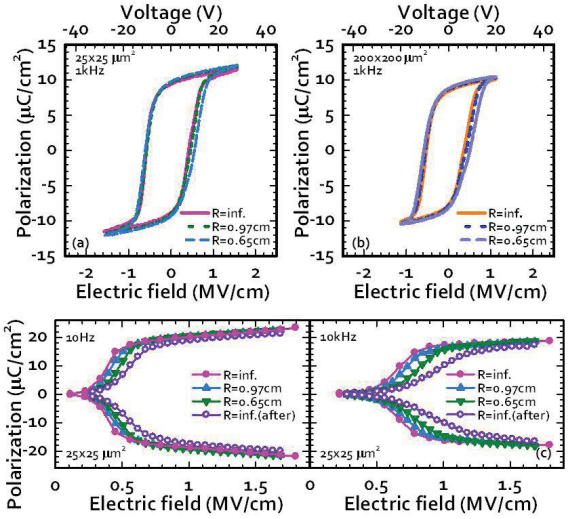

Fig. 7. Comparisons of the *P*-*E* characteristics of the fabricated capacitors with the size of (a) 25×25 μm^2 and (b) 200×200 μm^2 when the *R* was varied to ∞, 0.97 and 0.65 cm. For the case of 25×25 μm^2-sized capacitor, the polarizarization saturation behaviors were investigated at the signal frequencies of 10 Hz and 10 kHz when the *R* was varied to ∞, 0.97, 0.65 cm and restored to initial ∞ state.

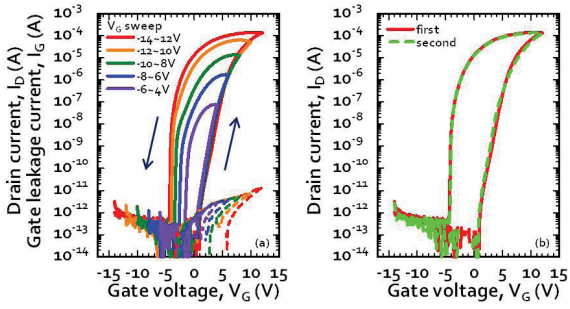

Fig. 8. (a) Sets of I_D-V_G transfer curves and gate leakage currents of the fabricated nonvolatile plastic memory TFT fabricated on the PEN substrate when the V_G sweep ranges were varied. (b) Variations of transfer characteristics of the same device between the first and the second sweeps in V_G. The V_D was set to be 5 V. The channel width and length of the evaluated device was 40 and 20 μm, respectively.

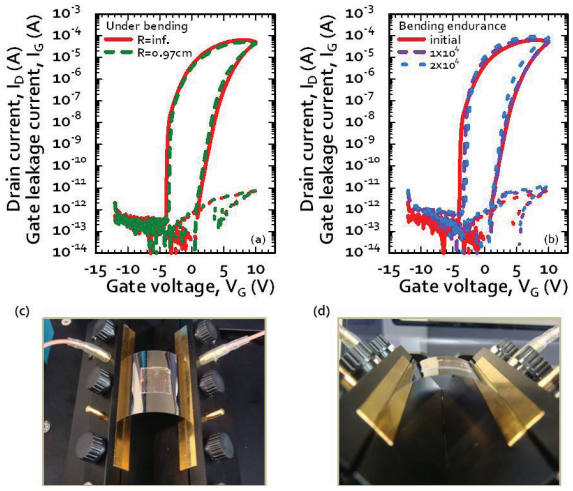

Fig. 9. Variations of transfer charactristics and memory behaviors of the fabricated plastic memory TFT (a) under the substrate bending situation with *R* of 0.97 cm and (b) after the 20,000 cycles of repetitive bending operations with the *R* of 2.35 cm. (b) Typical photo images of the bending fatigue evaluation performed by a specially-designed bending machine.

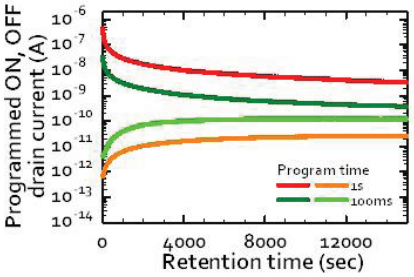

Fig. 10. Data retention behaviors of the fabricated plastic memory TFT as the changes in programmed I_D with a lapse of 15,000 s. The *on* and *off* states were programmed by applying the voltage pulses of 6 and -8 V, respectively. The pulse width was varied to 1 s and 100 ms.

almost disappeared during the retention phase. Although it was sufficiently encouraging to confirm the practical *on*/*off* ratio of higher than 2-orders-of magnitude for the fabricated plastic memory TFT even after a lapse of 4 hours, the programming and retention behaviors should be much more improved for real applications. The remaining issues and feasible appropriate solutions will be discussed in the next section.

5. Remaining issues

In previous sections, the promising methodologies and technical feasibilities were described for utilizing our proposed plastic memory TFTs prepared on the PEN substrate as core

memory devices for the future large-area flexible electronics. However, some technical issues remain to meet the required specifications. The first one is that the memory device reliabilities, especially data retention, were not so satisfying at this stage. The typical retention times of the previously reported memory TFT employing the polymeric ferroelectric GI and oxide channel are still in the range of several hours even when they were fabricated on the glass substrate (Lee K. H. et al., 2009a; Noh S. H. et al., 2007; Park C. H. et al., 2009). Three significant factors that critically affect the retention behaviors are intrinsic depolarization field, gate leakage components, and interface quality. The detailed features and solutions for each factor can be retrieved in our previous article (Yoon S. M. et al., 2011a). Considering the feasible applications utilizing the proposed flexible memory TFT, it is not necessary to guarantee years-of retention time. However, the stability of the stored data during several days will surely expand the application fields of the proposed flexible nonvolatile memory TFT. The second issue is that the obtained programming characteristics were sensitively dependent on the pulse width. Furthermore, the required duration for the stable programming was observed as long as 1 s, which has also been reported in other publications on the polymeric ferroelectric GI-based memory TFTs (Choi C. W. et al., 2008; Lee K. H. et al., 2009b; Uni K. N. N. et al., 2004). These properties have a direct influence on the programming speed of the flexible memory device. The discussions on the programming speed was also intensively discussed in our previous publication (Yoon S. M. et al., 2010d). Two remaining issues mentioned above are closely related to each other, because the long-time programming is definitely preferable to obtain the longer retention time. This is a kind of a severe trade-off. We have recently confirmed that the establishment of dual-gate configuration can be one of the most promising solutions to improve both requirements of the programming speed and data retention (Yoon S. M. et al., 2011b). Although the polymeric ferroelectric material was fixed in this work, it can be also possible to enhance overall performances of device by employing a new ferroelectric material. We sure that the programming and memory behaviors of the fabricated plastic memory TFT will be much improved by developing the suitable methodologies from now on.

6. Conclusion

In this work, we proposed and demonstrated the plastic nonvolatile memory TFT employing the ferroelectric copolymer gate insulator and oxide semiconductor active channel as a memory component for the flexible-type electronic devices. The device structure was designed to be Au/150 nm P(VDF-TrFE)/6 nm Al_2O_3/10 nm ZnO/Ti/Au/Ti/PEN. Firstly, the sound ferroelectric characteristics of the fabricated flexible P(VDF-TrFE) capacitors were well confirmed, that was of important in that they could be obtained with fully lithography-compatible process even on the PEN substrate at the temperature as low as 150 °C. The basic properties such as P_r, E_c, and polarization saturation behaviors with the increase in E were observed to not be so markedly varied with the changes in the R under the substrate bending situations. Then, the memory characteristics of the fabricated plastic memory TFTs with W/L of 40/20 μm were also evaluated, in which a 3.4 V memory window and 8-orders-of magnitude on/off ratio were successfully obtained. These characteristics did not experience so marked degradations at the bending situation with R of 0.97 cm and after the repetitive bending of 20000 cycles. We can conclude from the obtained results that our proposed hybrid plastic memory TFT can be a suitable candidate for an embeddable memory device

to realize the low-cost flexible electronic applications. However, as future works, the bending characteristics of the device will be more systematically investigated when the devices are bent with smaller *R*, which provides useful insights to design the flexible memory TFTs with excellent performances. The enhancements in programming and retention behaviors are also demanding for various flexible applications.

7. References

Aizawa, K. et al. (2004). Impact of HfO_2 buffer layers on data retention characteristics of ferroelectric-gate filed-effect transistors. *Applied Physics Letters*, Vol. 85, 3199-3201.

Baeg, K. J. et al. (2010). Controllable Shifts in Threshold Voltage of Top-Gate Polymer Field-Effect Transistors for Applications in Organic Nano Floating Gate Memory. *Advanced Functional Materials*, Vol. 20, 224-230.

Cho, B. et al. (2010) Electrical characterization of organic resistive memory with interfacial oxide layers formed by O_2 plasma treatment. *Applied Physics Letters*, Vol. 97, 063305.

Choi, C. W. et al. (2008). Comparative electrical bistable characteristics of ferroelectric poly(vinylidene fluoride-trifluoroethylene) copolymer based nonvolatile memory device architectures. *Applied Physics Letters*, Vol. 93, 182902.

Chu, L. W. et al. (2010). Design of Analog Pixel Memory Circuit with Low Temperature Polycrystalline Silicon TFTs for Low Power Application. *Symposium on Information Display Tech. Dig*. pp.1363-1366.

Forrest, S. R. (2004). The path to ubiquitous and low-cost organic electronic appliances on plastic. *Nature*, Vol. 428, 911-918.

Furukawa, T. (1989). Ferroelectric properties of vinylidene fluoride copolymers. *Phase Transition*, Vol. 18, 143-211.

Furukawa, T.; Nakajima, T. & Takahashi, Y. (2006). Factors Governing Ferroelectric Switching Characteristics of Thin VDF/TrFE Copolymer Films. *IEEE Transactions on Dielectrics and Electrical Insulation*, Vol. 13, 1120-1131.

Furukawa, T. et al. (2009). Ferroelectric switching dynamics in VDF-TrFE copolymer thin films spin coated on Si substrate. *Journal of Applied Physics*, Vol. 105, 061636.

Gelinck, G. H. & Leeuw, D. M. (2004). Flexible active-matirx displays and shift registers based on solution-processed organic transistors. *Nature Materials*, Vol. 3, 106-110.

Graz, I. M. & Lacour, S. P. (2009). Flexible pentacene organic thin film transistor circuits fabricated directly onto elastic silicone membranes. *Applied Physics Letters*, Vol. 95, 243305.

Horiuchi, T. et al. (2010). Lowered operation voltage in $Pt/SBi_2Ta_2O_9/HfO_2/Si$ ferroelectric-gate field-effect transistors by oxynitriding Si. *Semiconductor Science and Technology*, Vol. 25, 055005.

Hoshino, K. et al. (2009) Constant-Voltage-Bias Stress Testing of a-IGZO Thin-Film Transistors. *IEEE Transaction Electron Devices*, Vol. 56, 1365-1370.

Ishida, K. et al. (2010). User Customizable Logic Paper (UCLP) with Organic Sea-of-Transmission-Gates (SOTG) Architecture and Ink-Jet Printed Interconnects. *IEEE International Solid-State Circuits Conference Tech. Dig.*, pp. 138-139.

Ito, D. et al. (2003). Ferroelectric properties of $YMnO_3$ epitaxial films for ferroelecric-gate field-effect transistors. *Journal of Applied Physics*, Vol. 93, 5563-5567.

Jeong, J. K. et al. (2008). Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. *Applied Physics Letters*, Vol. 93, 123508.

Ji, Y. et al. (2010). Stable Switching Characteristics of Organic Nonvolatile Memory on a Bent Flexible Substrate. *Advanced Materials*, Vol. 22, 3071-3075.

Jung, M. et al. (2010). All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils. *IEEE Transaction Electron Devices*, Vol. 57, 571-580.

Kang, S. J. et al. (2008). Spin cast ferroelectric beta poly(vinylidene fluoride) thin films via rapid thermal annealing. *Applied Physics Letters*, Vol. 92, 012921.

Kang, S. J. et al. (2009). Non-volatile Ferroelectric Poly(vinylidene fluoride-co-trifluoroethylene) Memory Based on a Single-Crystalline Tri-isopropylsilylethynyl Pentacene Field-Effect Transistor. *Advanced Functional Materials*, Vol. 19, 1609-1616.

Kang, S. J. et al. (2009). Printable Ferroelectric PVDF/PMMA Blend Films with Ultralow Roughness for Low Voltage Non-Volatile Polymer Memory. *Advanced Functional Materials*, Vol. 19, 2812-2819.

Kim, K. H. (1998). Metal-ferroelectric-semiconductor (MFS) FET's using $LiNbO_3$/Si(100) structures for nonvolatile memory applications. *IEEE Electron Device Letters*, Vol. 19, 204-206.

Lee, K. H. et al. (2009). High-Mobility Nonvolatile Memory Thin-Film Transistors with a Ferroelectric Polymer Interfacing ZnO and Pentacene Channels. *Advanced Materials*, Vol. 21, 4287-4291.

Lee, K. H. et al. (2009). Flexible low voltage nonvolatile memory transistors with pentacene channel and ferroelectric polymer. *Applied Physics Letters*, Vol. 94, 093304.

Lee, M. J. et al. (2009). Low-Temperature-Grown Transition Metal Oxide Based Storage Materials and Oxide Transistors for High-Density Non-volatile Memory. *Advanced Functional Materials*, Vol. 19, 1587-1593.

Lee, N. Y. et al. (2003). Material design schemes for single-transistor-type ferroelectric memory cells using Pt/$(Bi,La)_4Ti_3O_{12}$/ONO/Si structures. *Japanese Journal of Applied Physics*, Vol. 42, 6955-6959.

Lee, S. et al. (2009). Resistive switching characteristics of ZnO thin film grown on stainless steel for flexible nonvolatile memory devices. *Applied Physics Letters*, Vol. 95, 262113.

Leong, W. L. et al. (2008). Non-Volatile Organic Memory Applications Enabled by In Situ Synthesis of Gold Nanoparticles in a Self-Assembled Block Copolymer. *Advanced Materials*, Vol. 20, 2325-2331.

Li, J. et al. (2010). A low-temperature crystallization path for device-quality ferroelectric films. *Applied Physics Letters*, Vol. 97, 102905.

Li, T. et al. (2003). The thermal stability of one-transistor ferroelectric memory with Pt-$Pb_5Ge_3O_{11}$-Ir-Poly-SiO_2-Si gate stack, *IEEE Electron Device Letters*, Vol. 50, 2280-2282.

Lim, S. H.; Rastogi, A. C. & Desu, S. B. (2004). Electrical properties of metal-ferroelectric-insulator-semiconductor structures based on ferroelectric polyvinylidene fluoride copolymer film gate for nonvolatile random access memory application. *Journal of Applied Physics*, Vol. 96, 5673-5682.

Lin, C. M.; Shih, W. C. & Lee, J. Y. (2009). Electrical characteristics of metal-ferroelectric ($BiFeO_3$)-insulator (Y_2O_3)-semiconductor capacitors and field-effect transistors. *Applied Physics Letters*, Vol. 94, 142905.

Lin, K. L. & Jain, K. (2009). Design and Fabrication of Stretchable Multilayer Self-Aligned Interconnects for Flexible Electronics and Large-Area Sensor Arrays Using Excimer Laser Photoablation. *IEEE Electron Device Letters*, Vol. 30, 14-16.

Ma, L. et al. (2002). Organic electrical bistable devices and rewritable memory cells. *Applied Physics Letters*, Vol. 80, 2997-2999.

Ma, L.; Xu, Q. & Yang, Y. (2004). Organic nonvolatile memory by controlling the dynamic copper-ion concentration within organic layer. *Applied Physics Letters*, Vol. 84, 4908-4910.

Matsumoto, A. et al. (2007). Ferro- and piezoelectric properties of vinylidene fluoride oligomer thin film fabricated on flexible polymer film. *Applied Physics Letters*, Vol. 90, 202906.

Nalwa, H. S. (1995) *Ferroelectric Polymers: Chemistry, Physics and Applications*, Marcel Dekker.

Naber, R. C. G. et al. (2005). High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Materials*, Vol. 4, 243-248.

Naber, R. C. G. et al. (2005). An Organic Field-Effect Transistor with Programmable Polarity. *Advanced Materials*, Vol. 17, 2692-2695.

Nguyen, C. A. et al. (2008). Enhanced organic ferroelectric field effect transistor characteristics with strained poly(vinylidene fluoride-trifluoroethylene) dielectric. *Organic Electronics*, Vol. 9, 1087-1092.

Noh, S. H. et al. (2007) ZnO-based nonvolatile memory thin-film transistors with polymer dielectric/ferroelectric double gate insulators. *Applied Physics Letters*, Vol. 90, 253504.

Nomura, K. et al. (2004). Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature*, Vol. 432, 488-492.

Novak, M. et al. (2010). Flexible copper-7,7,8,8 tetracyanochinodimethane memory devices-Operation, cross talk and bending. *Thin Solid Films*, Vol. 518, 2222-2227.

Osada, T. et al. (2010). Development of Liquid Crystal Display Panel Integrated with Drivers Using Amorphous In-Ga-Zn-Oxide Thin Film Transistors. *Japanese Journal of Applied Physics*, Vol. 49, 03CC02.

Ohara, H. et al. (2010). 4.0-inch Active-Matrix Organic Light-Emitting Diode Display Integrated with Driver Circuits Using Amorphous In-Ga-Zn-Oxide Thin-Film Transistors with Suppressed Variation, *Japanese Journal of Applied Physics*, Vol. 49, 03CD02.

Park, C. H. et al. (2009) Enhancing the retention properties of ZnO memory transistor by modifying the channel/ferroelectric polymer interface. *Applied Physics Letters*, Vol. 95, 153502.

Park, J. S. et al. (2009). Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors. *Applied Physics Letters*, Vol. 95, 013503.

Park, S. H. et al. (2009). Transparent and Photo-stable ZnO Thin-film Transistors to Drive an Active Matrix Organic-Light-Emitting-Diode Display Panel. *Advanced Materials*, Vol.21, 678-682.

Roh, J. et al. (2010) $PbZr_xTi_{1-x}O_3$ Ferroelectric Thin-Film Capacitors for Flexible Nonvolatile Memory Applications. *IEEE Electron Device Letters*, Vol. 31, 1017-1019.

Sekitani, T. et al. (2009). Stretchable active-matrix organic light-emitting diode display using printable elastic conductors. *Nature Materials*, Vol. 8, 494-499.

Sekitani, T. et al. (2009). Printed Nonvolatile Memory for a Sheet-Type Communication System. *IEEE Transaction Electron Devices*, Vol. 56, 1027-1035.

Seo, J. W. et al. (2009). Transparent flexible resistive random access memory fabricated at room temperature. *Applied Physics Letters*, Vol. 95, 133508.

Shih, W. C.; Kang, K. & Lee, J. Y. (2007). The improvement of retention time of metal-ferroelectric ($PbZr_{0.53}Ti_{0.47}O_3$)-insulator (Y_2O_3)-semiconductor transistors by surface treatments. *Applied Physics Letters*, Vol. 91, 232908.

Schroeder, R.; Majewski, L. A. & Grell, M. (2004). All-organic permanent memory transistor using an amorphous, spin-cast ferroelectric-like gate insulator. *Advanced Materials*, Vol. 16, 633-636.

Someya, T. et al. (2005). Integration of organic FETs with organic photodiodes for a large area, flexible, and lightweight sheet image scanners. *IEEE Transaction Electron Devices*, Vol. 52, 2502-2511.

Tokumitsu, E.; Nakamura, R. & Ishiwara, H. (1997). Nonvolatile Memory Operations of Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FET's Using PLZT/STO/Si(100) Structures. *IEEE Electron Device Letters*, Vol. 18, 160-162.

Tokumitsu, E.; Fujii, G. & Ishiwara, H. (1999). Nonvolatile ferroelectric-gate field-effect transistors using $SrBi_2Ta_2O_9$/Pt/$SrTa_2O_6$/SiON/Si structures. *Applied Physics Letters*, Vol. 75, 575-577.

Ueda, N. et al., (2010). A Novel Multi-level Memory in Pixel Technology for Ultra Low Power LTPS TFT-LCD. *Symposium on Information Display Tech. Dig.* pp.615-618.

Uni, K. N. N. et al. (2004). A nonvolatile memory element based on an organic field-effect transistor. *Applied Physics Letters*, Vol. 85, 1823-1825.

Wang, W.; Shi, J. & Ma, D. (2009). Organic Thin-Film Transistor Memory With Nanoparticle Floating Gate. *IEEE Transaction Electron Devices*, vol. 56, 1036-1039.

Yoon, S. M.; Tokumitsu, E. & Ishiwara, H. (1999). Adaptive-learning neuron integrated circuits using metal-ferroelectric ($SrBi_2Ta_2O_9$)-semiconductor (MFS) FET's. *IEEE Electron Device Letters*, Vol. 20, 526-528.

Yoon, S. M. et al. (2009). Effect of ZnO channel thickness on the device behaviour of nonvolatile memory thin film transistors with double-layered gate insulators of Al_2O_3 and ferroelectric polymer. *Journal of Physics D*, Vol. 42, 245101.

Yoon, S. M. et al. (2009). Effects of Chemical Treatments on the Electrical Behaviors of Ferroelectric Poly(vinylidene fluoride-trifluoroethylene) Copolymer for Nonvolatile Memory Device Applications. *Japanese Journal of Applied Physics*, Vol. 48, 09KA20.

Yoon, S. M. et al. (2010). Impact of interface controlling layer of Al_2O_3 for improving the retention behaviors of In-Ga-Zn oxide-based ferroelectric memory transistor. *Applied Physics Letters*, Vol. 96, 232903.

Yoon, S. M. et al. (2010). Fully Transparent Non-volatile Memory Thin-Film Transistors Using an Organic Ferroelectric and Oxide Semiconductor Below 200 °C. *Advanced Functional Materials*, Vol. 20, 921-926.

Yoon, S. M. et al. (2010). Nondestructive Readout Operation of Oxide-Thin-Film-Transistor-Based 2T-Type Nonvolatile Memory Cell. *IEEE Electron Device Letters*, Vol. 31, 138-140.

Yoon, S. M. et al. (2010). Characterization of Nonvolatile Memory Behaviors of Al/Poly(vinylidene fluoride.trifluoroethylene)/Al_2O_3/ZnO Thin-Film Transistors. *Japanese Journal of Applied Physics*, Vol. 49, 04DJ06.

Yoon, S. M. et al. (2011). Nonvolatile Memory Thin-Film Transistors using Organic Ferroelectric Gate Insulator and Oxide Semiconducting Channel. *Semiconductor Science and Technology*, Vol. 26, 034007.

Yoon, S. M. et al. (2011). Oxide Semiconductor-Based organic/Inorganic Hybrid Dual-Gate Nonvolatile Memory Thin-film Transistor. *IEEE Transaction Electron Devices* (To be published)

Zschieschang, U. et al., (2010). Flexible Low-Voltage Organic Transistors and Circuits Based on a High-Mobility Organic Semiconductor with Good Air Stability. *Advanced Materials*, Vol. 22, 982-985.

10

Use of FRAM Memories in Spacecrafts

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1. Introduction

This chapter shows some applications of commercial ferroelectric memories in the space. The discussion goes through the description of the theory behind their usage in this environment and describes the techniques used to achieve the desired reliability in real designs.
We are focusing on the *low-Earth orbit*, or LEO, the zone surrounding the Earth between $500 \div 800$ km, characterized by many challenging aspects, mainly related to the reduced atmosphere. Indeed the biggest problem of this environment is given by the presence of high-energy particles (not filtered by atmosphere and the Van Allen belts) hitting the active areas of electronic devices. These particles are thus reducing the reliability of the integrated circuits (i.e., their life or the life of information stored in them), affecting the reliability of the complete space-borne mission.
Other issues are related to the reduced cooling effect due to the lack of air convection movements: electronic systems have to reduce at most the power consumption, in order to decrease the power to be dissipated. Both power consumption and heat dissipation can be achieved using commercial low-power devices and low-power techniques (i.e., power cycling, smart power management policies, ...).
We motivate the use of FeRAM memories and propose some architectural solutions which can mitigate the effects of cosmic rays, without using expensive radiation-hardened space components. The choice of using commercial-off-the-shelf components (COTS) improves the overall characteristics of the whole avionic system, since it helps reducing its costs, reducing the power consumption (and so the power to be dissipated in the environment) and increases the re-usability of existing projects and documentation.
We applied our considerations and techniques to some small satellites developed in our research group during the last years. We cover two main projects: the first is a small prototype which was designed few years ago and launched in 2006; the second is a more advanced and challenging project aimed at developing a modular platform for small-sized satellites, which is still on-going. Both of them contain FeRAM devices and we show here how these devices have been introduced and how they can actually increase the global avionic performance and reliability. We discuss which are our constraints on the functional and architectural point of view (memory size, power consumption, latency, reliability) and which are the reasons for using FeRAM memories in our applications. In both designs we have performed simulation of the chip behavior in space through some space simulation environments (i.e., SPENVIS, CREME) to analyze the reliability of our design in this environment.
At the end we draw some conclusions on the work done and on the results we have, tracing further steps and considerations for future applications.

2. Technical background: the FeRAM cell

The idea of using ferroelectric materials to store digital data dates back to 1952, but it was practically implemented only starting from the 80s. The ferroelectric RAM cell, known as FeRAM or FRAM, is conceptually similar to the DRAM cell, in that a single capacitor stores one bit of information and the cell is connected to a memory column via a single pass transistor (1T-1C cell, although 2T cells are also common). The big difference lies in the dielectric of the storage capacitor: while DRAM cells use a layer of standard linear material, the dielectric of a FeRAM cell is made of ferroelectric material, usually PZT (lead zirconate titanate).
Using a ferroelectric dielectric makes the cell behave very differently from a DRAM cell, for several reasons. On one side, the dielectric constant of ferroelectric materials is very high, so that it is possible to create larger capacitors in a small space; on the other, the material exhibits two stable polarization conditions and it is possible to switch between them by means of applying an electric field of different polarity. The polarization will be kept after removing the applied field, so that it is possible to link the polarization state to a logic state and that state will be maintained also in absence of power supply. This means that the FeRAM cell is non volatile and that no refresh is necessary to keep the information in the memory.
Going a bit more into details, while in a DRAM cell the capacitor has one of the electrodes grounded, in the FeRAM cell the corresponding electrode is connected to a so-called driveline. During a write cycle the driveline (dl) is driven to complementary voltage with respect to the bitline (bl): $bl = 0\,\mathrm{V} \rightarrow dl = V_{dd}$; $bl = V_{dd} \rightarrow dl = 0\,\mathrm{V}$. In this way it is possible to provide positive electric field to write a 1 and negative field to write a 0, without need for dual polarity supply voltage.
Like for DRAMs, the reading process is destructive: it is not possible to read the contents of a cell without actually clearing it, because of the way the information is stored in the device. To know which of the two possible polarization states the dielectric holds, the only way consists in writing a new value to the cell with the bitline pre-charged but in high impedance state. Depending on the previous polarization of the cell, this process will or will not produce a voltage pulse out of the bitline.
For our purposes, there is no need to go into further details of the process, the key issue is that the information in the cell is not related to the charge stored in the capacitor but to the polarization of the dielectric.
Read and write cycles require basically the same operations and can both be completed in times in the order of tens of nanoseconds.

3. Technical background: Heavy ions and total dose

When selecting components for space missions, the key issue is reliability. Electronic systems designed for spacecrafts are normally built using space qualified components. These devices undergo special treatment to conform to specs identical or similar to MIL standards.
Regular commercial, military or scientific space missions from national or international space agencies have budgets allowing the designers to work only with space qualified components, but in the last few years many universities successfully completed and launched small satellites built using commercial-off-the-shelf (COTS) components. Their choice was mainly driven by having budgets several orders of magnitude smaller than those of regular spacecrafts.
Special considerations have to be taken when selecting COTS components for space missions. Let's analyze the main point to take care of:

- radiation: at ground level, the atmosphere constitutes an effective shield to incoming space radiations. Outside the atmosphere the radiation levels are much higher and impose severe limitations on electronics. We will evaluate them in details in the following.
- pressure: no atmosphere is present in orbit. This fact creates two main consequences: pressure is very low and power dissipation through convection is impossible. The low pressure limits the use of devices with liquid components (like electrolytic capacitors) and it is necessary to check that the packages of electronic components do not emit dangerous gases and do not break during depressurization phase, so outgassing and offgassing tests are necessary. Power dissipation limitations are not normally of concern for low power devices like memories.
- temperature: even if outside temperature can be extreme in light and in darkness, inside small satellites it can be demonstrated that temperature is not a big concern. Temperature remains in the range $-10\,^{\circ}\mathrm{C}$ to $20\,^{\circ}\mathrm{C}$, so normal devices rated for automotive use are well suited for operation inside a satellite (at least relating to this parameter).
- vibration: heavy vibrations are normal during the launch phase of the mission. Again, automotive devices are normally designed to sustain this vibration level.

At the moment there are no FeRAM devices conforming to space specs, but it is possible to obtain components graded for the automotive market. The main concern in using such devices is the radiation environment, while the other specs are reasonably met.
Radiation in space comes from different sources. The Sun is the main emitting body to be considered, but also background cosmic rays have to be taken into account. The electromagnetic field of the Earth plays a significant role in shielding incoming particles, so that radiation levels will be different depending on the orbital parameters of the spacecraft.
Solar flares and 11 years solar emission cycle have to be carefully considered, but plenty of data was accumulated during years of space activities, so that now we have a good characterization of the radiation environment around the Earth and it is possible to know the exposure levels for a specific space mission with a high level of confidence (see for example SPENVIS).
The damages produced by the incoming radiation can be divided in two categories: cumulative effects of the dose received, known as TID or Total Ionizing Dose, and effects of a single particle hitting the device, named SEE, Single Event Effects (for a more comprehensive introduction see NASA-Gsfc (2000)).
Total dose accounts for a degradation of the performances of the transistors (MOSFETs and BJTs). In particular, on MOSFET devices the main problem comes from a gradual shift in the threshold voltage. Above a certain TID this threshold shift is so high that the transistor cannot switch anymore, causing a functional failure of the circuit. TID is measured in $\mathrm{krad(Si)}$. It is relatively simple to test the behavior of a device for TID. X-ray apparatuses derived from those used in medical applications suitable for the scope are available at a relatively low cost.
Single events create several failures depending on the device involved, the technology and other conditions. The particles responsible for SEE are mainly heavy ions and protons. When a high energy particle hits the surface of a silicon chip, part of its energy is transferred to the chip as electric charge (secondary electrons emission). The amount of energy transferred is called LET (Linear Energy Transfer), measured in $\mathrm{MeV\,cm^2\,mg^{-1}}$.
The main effects are:

- Single Event Upset (SEU): this is a recoverable error that appears in memory devices. The impacting particle hits the sensible area of a storage device, for example the capacitor of a DRAM cell, and transfers an amount of charge sufficient to alter the contents of the

memory. This damage is called a soft error, meaning that the damage is not permanent and it is sufficient to rewrite the memory to restore correct behavior.

- Single Event Latch-up (SEL): this is a potentially destructive error typical of CMOS circuits. The structure of a complementary gate in CMOS logic contains a parasitic PNPN device, similar to an SCR, which is not operated under normal conditions, but can be triggered by a high energy particle hitting the gate of the SCR device. Once triggered, the SCR remains ON until the power supply is switched off. When this device is on, it creates a low resistance path between power supply and ground. The current can be very high, creating an hot spot in the device that can in turn permanently damage it.
- Single Event Functional Interrupt (SEFI): it is defined as erratic behavior of a complex circuit due to the consequences of the impact of a single particle. It is similar to SEU, but the affected area, instead of being a simple memory cell, is a FSM or other sequential circuit which is forced into an unwanted state by the event. The error may persist until the next reset or may be recovered at some time. In the case of a memory device, a SEFI occurring in the control part of the device can lead to reprogramming a big area of the matrix (typically a whole row).
- Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB): these damages occur when a particle hits the active area of a power MOSFET transistor under certain bias conditions, creating a physical damage, such as oxide breakdown for SEGR, overheating due to large currents for SEB, that prevents normal operation of the device. Low power devices such as memories are not subject to SEB, but SEGR has been reported if a particle hits a EEPROM or Flash memory during the erase procedure, due to the relatively high voltages used during such operation.

Testing one device for SEE typically includes exposing it to a precise flux of particles, generally heavy ions, characterized by a specific LET, for a specified amount of time. The number of detected errors allows the determination of the device sensitive area, or cross-section, at the ions' LET. This procedure has to be repeated for different LETs, so that a graph showing the cross-section of the device as a function of the LET can be derived. This process is very expensive because this kind of tests can only be performed in a cyclotron. Alternative lower cost methods include the use of laser pulses or small radioactive sources based on Californium 252 which emits heavy ions of different LET, but in this case it is difficult to relate test results to more rigorous cyclotron methods.
Once a device is characterized for TID and SEE behavior, knowing the expected radiation environment at the programmed orbit, it is possible to predict which errors can be expected during operation and what is the relevant error rate.

4. FeRAM strengths

In the previous sections we have introduced the FeRAM technology and described the challenges posed by the space environment.
What are the advantages of using FeRAM devices in space subsystems? The three main design parameters of the electronic systems of small satellites are power consumption, physical dimensions and radiation environment behavior. Let's evaluate the first two items: the electric power in the satellite comes from solar panels, which are necessarily of small dimensions, leading to few watts of average power to cover all the satellite's functions, so it is necessary to make the best use of any mW of available power. Launch costs are directly proportional to the mass of the system, so it is mandatory to reduce as much as possible dimensions and mass of the electronic systems.

As previously stated, FeRAM memories are RAM devices, meaning that read and write procedures do not differ significantly and random write is possible without the need of a previous erase of a cell, but they are also non volatile, so that information is not lost after removing power supply.
We can therefore compare FeRAM memories both to RAMs and Flash devices. It is possible to note that in principle the structure of the FeRAM memory cell is very similar to the DRAM one, but, not relying on the charge in the capacitor, it does not request the refresh procedure, which is time and power consuming. In fact in DRAM devices most of the power is used by the refresh procedure. FeRAM cells are bigger than DRAMs, so it is not possible to use FeRAM memories to store huge amount of data. Today's top density is 128 Mibit per chip (prototype by Toshiba, Shiga et al. (2010)) but most of the available devices are in the 1 to 8 Mibit range (RAMTRON). This is probably more a problem of amount of financial investments in this technology than of intrinsic limitations of the ferroelectric capacitor used in the cell. In any case, memory requirements of small satellites are normally compatible with the size of available FeRAM devices, except for imaging payloads if local storage of a certain number of images is mandatory.
The most interesting application of our technology is however evident when comparing with Flash or EEPROM devices. Read operations in FeRAM and Flash devices are equivalent both in speed and power requirements. Write operations on a Flash memory are quite complex. The first phase consists in a page erase, which takes a time in the order of tens of milliseconds, followed by a write operation of the new values. Even to rewrite a byte, one full page has to be erased and the unmodified cells have to be rewritten in place. The erase procedure requires a high supply voltage (negative for erase, positive for write) which is internally generated by the device using a charge pump circuit. EEPROM devices can be reprogrammed on a single byte basis, speeding up the write process when a single random byte has to be altered, but the need for high voltages is the same as for Flash devices and the operation can be completed in tens of microseconds. A comparison in power and speed can be found in Sheikholeslami & Gulak (2000), although a bit out of date. Another aspect to be considered is the device endurance. The number of write cycles that can be sustained by a Flash or EEPROM device is in the order of $1 \times 10^4 \div 1 \times 10^5$, while FeRAM memories can be written more that 1×10^{12} times, with 1×10^{16} cycles being claimed by TI and RAMTRON on new devices. The same drawback of lower device density noted above in the comparison with DRAMs is applicable to the comparison with Flash devices.
As a summary, FeRAM devices are attractive for use in small spacecrafts as a replacement for both RAM and Flash memories when the size of the memory is small, because of the ease of use, non volatility (when compared to RAM), the low power requirements, the speed advantage in the write process and the endurance, when comparing with Flash memories.
The last, but not least, point to take into consideration is the radiation behavior. Several tests performed on the FeRAM cells show that the SEU response is very good (Benedetto et al. (1999)), definitely better than the one of most Flash or DRAM devices, indicating that this technology is very appealing for space applications.

5. FeRAM weakness

The biggest obstacle at the moment in using FeRAM devices in spacecrafts is the lack of commercially available radiation hardened components. It is clear from the previous section that the memory cell has several advantages with respect to other non volatile competing technologies, but at the moment the only devices available off the shelf are from Ramtron and Fujitsu. There is almost no literature on heavy ions behavior of these chips, apart from a single

paper reporting SEU tests on Hynix devices (Hynix does not have any FeRAM device in its catalog nowadays) and Ramtron 256 Kibit and 64 Kibit memories (Scheick et al. (2004)). The results of these tests were disappointing: although no SEU was observed in the memory cells, there were errors involving several cells at a time. These errors are compatible with SEUs hitting the CMOS control logic of the array, triggering unwanted writes to the memory. This means that, even if the memory cell itself is immune or very resistant to heavy ions induced errors, this is not true for the surrounding logic built using a standard CMOS process.
It is possible to harden the memory control logic, either by using a rad-hard process or by hardening by design, as demonstrated for example in Kamp et al. (2005), but no such devices are commercially available at the moment.
TID behavior of Ramtron devices was tested by JPL and included in a report by Nguyen & Scheick (2001). The results are compatible with LEO orbit operations.
It is interesting to note that Fujitsu sells radiation resistant RF-ID modules that comprise a FeRAM memory for non volatile storage. Another product from the same manufacturer is a microcontroller featuring FeRAM as a substitute for both RAM and Flash memories. The device is not intended for operation in hostile environment.

6. Possible solutions

The problems highlighted in the previous section can be overcome in two different ways. The first is to design a FeRAM memory specifically for space applications, the second is to use COTS devices taking specific system design measures to prevent the failures due to the CMOS logic surrounding the memory array.
Obviously the first solution is preferable, but it involves high development and production costs and time, so it is not affordable when designing low cost spacecrafts such as university satellites.
In details, to create a rad-hard version of a FeRAM memory it is necessary to use a rad-hard CMOS process to build row and column decoders and the read/write control logic. Rad-hard processes normally use SOI (silicon on insulator) or SOS (silicon on sapphire) techniques. As an alternative, the addition of an epitaxial layer to the substrate of a standard CMOS process can lead to improved performances, at least about SEL sensitivity. Since it is not difficult to add a ferroelectric layer to a rad-hard CMOS process, this way is feasible, but the associated costs are very high.
A variation on this subject is radiation hardening by design. An example of this technique is available in Philpy et al. (2003). Hardening by design does not require special processes but only following special design rules that improve radiation behavior of the device. This way is probably less expensive than using a rad-hard process, but it requires nevertheless the design of special components.
The alternative of using COTS devices is very attractive and is feasible in the case of FeRAM memories because of the characteristics of these devices.
Let us analyze more in details the problems of commercial devices and how to overcome them. As shown from the results of the tests performed by Scheick et al. (2004), the risks of data corruption or physical damage come from the standard CMOS logic surrounding the memory array. We have to improve the device sensitivity to SEL and to soft errors. TID is not a problem because the performance reported in Nguyen & Scheick (2001) is reasonable for LEO missions.
To prevent the risk of loss of the device due to latch-up, it is possible to monitor the supply current and to switch off the chip in case of overload, indicating SEL occurrence. This procedure has to be done very carefully in CMOS logic, because it is not normally sufficient

to remove power supply to be sure to reset the parasitic structure responsible for latch-up. The structure of the input circuitry of CMOS devices always includes clamp diodes, so even removing power supply it is possible to continue to supply the chip via inputs at logic high state.
SEL protection circuitry is mandatory when using COTS devices in space applications, so we developed an hybrid circuit that monitors supply current to a satellite subsystem, switches off power supply when a SEL is detected and sends an interrupt to the associated microcomputer to signal the event. Depending on the subsystem involved, the microcomputer can either cycle power supply to a complete portion of the satellite or insure in other ways that no signals at logic high state are connected to the subsystem affected by the SEL.
Soft errors are the second problem to address. The non volatility of the information stored in the FeRAM is a great help in this respect. Soft errors can only occur when the memory is powered, but our devices need power supply only when it is necessary to read or write information, not to maintain internal data. This suggests a strategy for SEU and SEFI effects mitigation: the device is powered only during read or write operations, switched off otherwise. This strategy is possible only if the memory stores data which are to be seldom read or written, not if the device is used to store the active CPU program. Our use of FeRAM memories falls indeed in the first case: our systems have microcontrollers equipped with internal memory for program and data, external memory is used only to store telemetry, statistics and backup configuration data and program. The duty cycle of power supply is therefore very low, and this ensures a drastic reduction of SEU/SEFI sensitivity. We adopt a second strategy for important data, such as the backup copy of processor program: we store separate copies on multiple devices, furthermore the data are associated with strong error detection CRC codes, so that it is possible to detect if what is stored in a device was corrupted by SEU/SEFI. Corrupted data are regenerated from the other copies so the system integrity can be guaranteed.
In the following sections we will present more details on our application and on the adopted solutions, together with an estimate of the reliability of our approach.

7. Design and analysis of commercial components in the space

After discussing some possible solutions to overcome the problem of using FeRAM components in the space, in the following sections we are detailing two examples of their usage taken from real-life applications developed in our research group. Both examples are using commercially available components and are exploiting some architectural solutions to mitigate the radiation effects on these devices.

7.1 The PiCPoT nano-satellite

In response to industry and academic research interests, in 2004 we started a design activity at Electronics Dept. in tight cooperation with our Aerospace Engineering Dept. and other departments of our University, aimed at developing and manufacturing a low-cost prototype of a fully operational nanosatellite. The design activity lasted three years, gathered about 10 people among professors and PhD students, plus about 20 undergraduate students (the former for the whole period, while the latter stayed for shorted period, between 6 and 12 months each).
After an effort of about 12 man-years (staff+student) for design, manufacturing and testing, we built a flight model and two engineering models of the PiCPoT satellite shown in Fig. 1.
The satellite has been completely designed using COTS devices, with the only exception of solar panels. It contains (see Fig. 2): five solar panels; six battery packs; three cameras

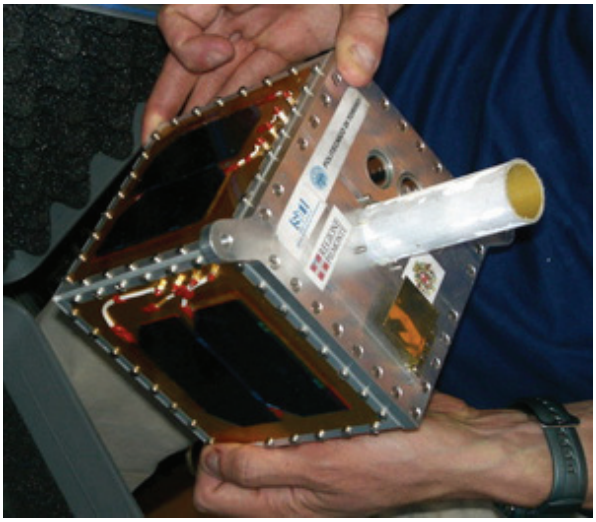

Fig. 1. The engineering model of PiCPoT

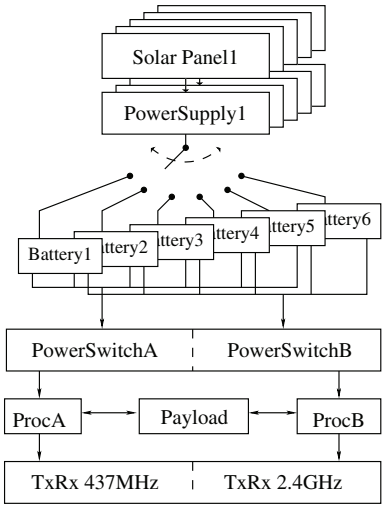

Fig. 2. PiCPoT internal structure

with different focal lengths; five processors in full redundancy; two RX-TX communication modules with antennas operating at 437 MHz and 2.4 GHz, respectively; six PCBs, all of them hosted in a cubic aluminum case, 13 cm in side. The radiation behavior of PiCPoT was carefully considered, because it is a rather complex system containing, as noted, 5 processors, different kind of memories and programmable logic devices.
In particular we divided the soft errors in the memory devices in three categories:

1. errors on dynamic data and/or in code segments resident in volatile memory;
2. errors on data stored in non-volatile memory;

3. errors on program code stored in non-volatile memory.

The outcome of such events may be wrong data, wrong behavior (if the event affects some data dependent control, for instance) or even a crash (i.e., if the upset results in a non-existent op-code for a processor).
There are several solutions to address this problem, each with its own advantages and shortcomings. Some cope with all three kind of errors, others do not address all of them. We applied different techniques in various parts of the satellite, depending on the kind of protection we wanted to provide. The selection was driven by the need to keep the design simple and power consumption and total budget low. Therefore we did not use radiation-hardened devices (too expensive and against the whole philosophy of the project to use COTS components wherever possible), nor memories with error correcting code (ECC), useful only for dynamic data and which do not protect against multiple bit upsets.
Even if no radiation-hardened components were used, the susceptibility of COTS components to radiation can be very different. Careful selection of the best devices for the application allows us to strongly reduce the probability of single event upsets.
We examined several kind of memories in search for the best ones, and in particular we considered:

- *Dynamic RAM* (DRAM): it is the most dense memory and it is used when large amount of memory is required. It is rather sensitive to radiations. Those parts of the satellite that depend on this kind of memory must be protected in some way.
- *Static RAM* (SRAM): it has been shown by Ziegler et al. (1996) that these are more sensitive to radiation than dynamic RAMs, but have the advantage of consuming less power. Processor registers also use the very same technology.
- *Flash*: Although the charge pump mechanism to reprogram a cell has been shown to be susceptible to TID effects, the cell proved to be robust against SEU, Miyahira & Swift (1998), because more energy is required to change the state of a bit compared to conventional RAM devices. For this reason, flash devices are more tolerant to radiation and are a good candidate for vital data and code.
- *Ferroelectric RAM* (FeRAM): Compared to flash memories, writing operations on an FeRAM can operate at lower voltages and are 2 to 3 order of magnitude faster. This allows saving energy and at the same time maintaining the good tolerance to radiation of flash devices. This technology looks promising for space applications but few information about the behavior of FeRAM in space is available in the literature.

We used a mix of all the above memories because strengths and weaknesses were often complementary. When available, data on radiation effects on memories was used to compare similar devices and select the best one. Dynamic and static memories were used for execution, while Flash and FeRAM were used for permanent data and program storage. Being highly experimental and having only a few documentation on their behavior, FeRAM was only used to hold non-vital data, such as the telemetry stream acquired from sensors.

7.2 Operation, timing, fault tolerance

The design of PiCPoT is aimed at high tolerance to faults and radiation effects while using only COTS components.
The whole design has been based on a redundant architecture we developed mixing both *hot* and *cold* redundancy techniques (Shooman (2001)). Architecture and operation are organized around a hot-redundant central *power management and timing unit*, that drives alternatively

two cold-redundant sub-satellites, called processing chain A and B, for housekeeping measurements (temperature, voltage, current), and a single payload board that controls the cameras. The two chains are switched on and off alternatively each minute to reduce the effects due to the presence of radiation.
The two sub-satellites have been developed by two different teams, using different components, in order to avoid the possibility of having the same technological or design issue on the two systems at the same time. One of the chains has been equipped with a ferroelectric RAM chip as main storage memory for telemetry data.

7.3 Design constraints

The design and the assembly of a satellite must abide tighter rules than usual "good and safe design" criteria applied for any electronic system. Moreover, the choice of using COTS components and technology, allowing failures at the device level, makes mandatory the adoption of design techniques which guarantee system operation, even in presence of limited failures.
The design constraints were those already mentioned in Sec. 3.
All mechanical and thermal specifications are easily met by integrated devices. Regarding cosmic rays, the planned orbit is close to the Van Allen belts, where a limited amount of heavy ions is present; these radiations may cause latch-up in CMOS devices and single-event upsets in memories. Due to the low orbit, total dose effects are limited.
As previously discussed, FeRAM devices are able to better cope with all these aspects since:

- This technology reduces the overall amount of energy required in normal operating mode with respect to Flash devices, so that the power to be dissipated is also reduced, allowing wider operating temperature conditions and improving the chip behavior in absence of air.
- The core memory requires lower operative voltages, the electromagnetic emissions are characterized by less energy and thus they are producing less interference in the satellite.
- The FeRAM cell is less radiation sensitive and thus it improves the overall behavior in presence of heavy ions.

7.4 Memory requirements

We selected the memory for the various subsystems of our satellite based on the following considerations.

7.4.1 Size

Knowing the amount of data we have to store is one of the main aspects when selecting a memory, reducing the number of available technologies and forcing several architectural clues in the overall project (as the the number of bit required to address it, the access speed, . . .).
In our case we had different kind of memory usages and thus different sizes required.
As a first issue we can identify two applications in our project: external memory in PiCPoT was used for storing telemetry data and for storing images (Passerone et al. (2008)). Obviously these two usages request different memory sizes and characteristics. Indeed, whilst for pictures we require a fairly big amount of data (usually some hundreds of kilobytes), for storing a telemetry history we only need few kilobytes. On the other hand, while loosing a part of an image can be negligible, or it can be tolerated, loosing telemetry data, thus loosing information on system behavior, can lead to difficult situations, especially in case of troubles. Table 1 is resuming these considerations.

Application	Memory Size	Available Tech.	Data loss
Telemetry	$(1 \div 10)$ kB	Flash, EEPROM, FeRAM	forbidden
Pictures	$(0.1 \div 1)$ MB	Flash, DRAM, SRAM	acceptable

Table 1. Memory size considerations.

7.4.2 Radiation tolerance

At the time we started the development of our satellite, a small number of studies had been published on the tolerance of commercial FeRAM components to the space environment, see Nguyen & Scheick (2001) and Scheick et al. (2004). Thanks to these works we were able to estimate the cross-section for the device chosen in our project. Comparing the cross-section with the data provided by SPENVIS, we verified the usability of such devices in space. Figure 3 provides the output data from the SPENVIS simulation, describing the total radiation dose for one year of activity. The worst case shielding inside our satellite is about 2 mm of aluminum.

Concerning TID, the studies mentioned above classified our devices as able to tolerate an exposure above 10 krad(Si) and the environmental simulation provided by SPENVIS was noting only 1 krad(Si) per year, so we were confident that our project was able to comply with our orbit without troubles.

At the time we developed our design, there was no direct SEU characterization for the device we selected, namely a Ramtron 25L256, 256 Kibit with SPI interface.

Therefore we tried to extrapolate the device cross-section considering the above published data and assuming similar performance from devices built using the same technology. Simulating the satellite orbit in LEO through SPENVIS we obtained the expected heavy ions flux, see Fig. 4. By using the estimated cross-section, we obtained in output an average SEU rate of 0.2 events/day. Moreover, we reduced the actual cross-section by powering off the device when not used. With a duty-cycle of 10 s/min, we are able to achieve an average SEU rate of one event per month, thus giving us a good reliability level for our application target (i.e., minimum mission time of three months).

7.5 Design strategies

Having demonstrated that a FeRAM device can fit our design target, we will now discuss how to improve, by using architectural solutions, the overall behavior of the memory when exposed to the space environment.

7.5.1 Reducing the single event latchup effects

Single event latch-up as exposed in Gray et al. (2001), or simply latch-up (LU), occurs when a parasitic SCR made by the couple of complementary MOS devices is turned on by high input voltages (this is the usual LU in ICs, caused for instance by input over-voltages) or by high energy particles which induce a small current (this is the case for a space device). The effect is a high, self-sustaining current flow, which can bring a high power dissipation and, in turn, device disruption.

LU-free circuits (latch-up cannot occur) can be designed by avoiding CMOS all-together, or by using radiation hardened technology; since one of the goals of PiCPoT is to explore the use of COTS components for space applications, we decided to keep only some critical parts LU-free by proper device selection, and to allow using standard CMOS devices in other circuits. These, however, must be LU-safe (latch-up can occur, but makes no harm), with specific protection circuits.

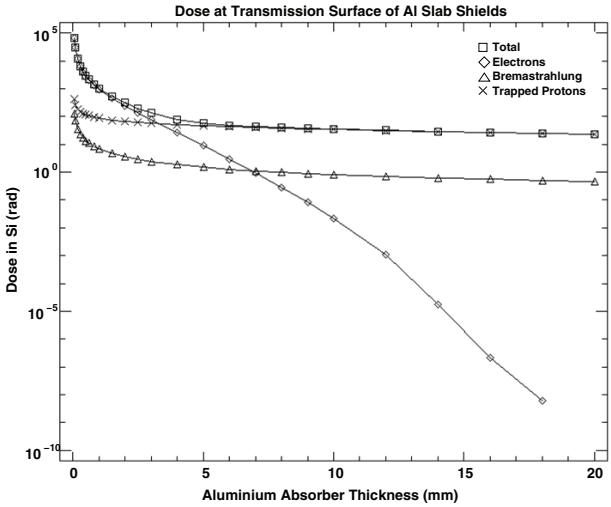

Fig. 3. Total dose radiation diagram with respect to the shield thickness in LEO orbit.

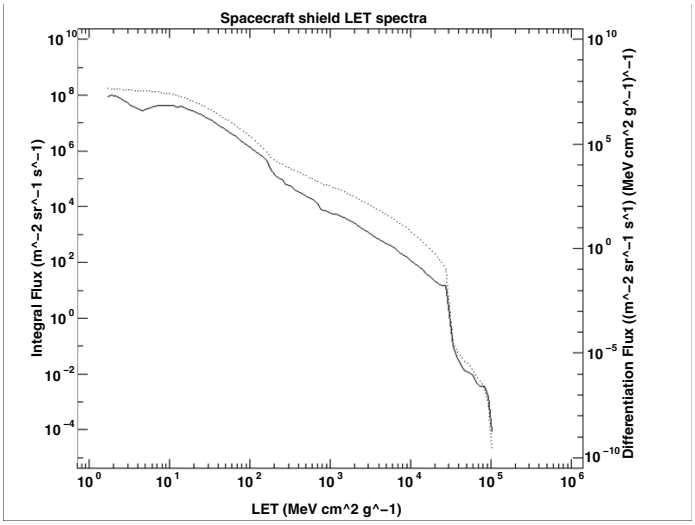

Fig. 4. Heavy ion flux vs. LET in LEO orbit.

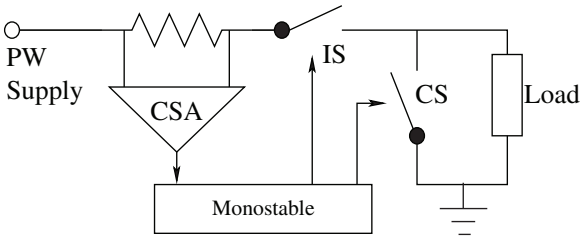

Fig. 5. Block diagram of latchup protection circuit.

The basic idea behind protection is to constantly measure current and to immediately turn the power off as soon as anomalous current consumption is detected. Once the transient event is over, normal operation can be restored. This technique is analogous to a watchdog timer, except that it actively monitors the circuit to be preserved, rather than waiting for the expiration of a deadline. Each supply path should have its own protection circuit, which should itself be LU-free, e.g. using only bipolar technology for its components.
The block diagram of the protection circuit of a single supply path is shown in Fig. 5, and includes:

- a current sense differential amplifier (CSA),
- a mono-stable circuit with threshold input,
- isolating and current-steering switches (IS and CS),

When the current crosses the limit set for anti-latch-up intervention (usually $2\times$ the maximum regular current), the mono-stable is triggered and isolates the load from the power sources for about 100 ms. To fully extinguish the LU, the shunt switch steers residual current away from the load.

7.5.2 Reducing the single event upset effects

One technique to approach the problem of SEU effects mitigation is to use redundancy. In general, at least three replicated units are necessary to implement a voting mechanism, where the majority wins and allows correction of a fault. The replicated unit can be a complete board (processor, memories and peripherals), a physical device on a board (three instances of the same component) or an abstract unit within a device (three memory segments in the same chip, holding identical information). This method potentially allows active identification of an SEU even in RAMs during the execution of a program, and to promptly act to correct it. However, the space available inside the satellite did not allow us to replicate identical boards (except for the system level duplications which are discussed in the remainder of this paper), or even devices within a board. Nonetheless, in some of the processor boards the program stored in Flash memory is maintained in multiple copies and a procedure to search for SEUs can be explicitly activated. Data, such as pictures or telemetry, on the other hand, are not protected and if an SEU occurs, the information downloaded to ground will simply be incorrect.
Since RAMs, both static and dynamic, including registers inside the processors, are the most sensitive devices to SEU, and they are not replicated, other techniques must be used to ensure proper behavior. Our solution is to periodically turn off processor boards and start a complete boot procedure. Given that the program is stored in flash memory (possibly with some duplication) and that RAMs go through a power cycle and reset, the soft error will be

completely eliminated. Clearly, data that have to persist for more than one power cycle have to be stored in some kind of non volatile memory.
Obviously, whatever command was being executed, a SEU will potentially result in wrong data or a crash. This however does not preclude the system to work correctly at the subsequent re-boot. The periodicity that was selected is 60 s: it allows smooth execution of all commands to be executed with a good margin. This technique is similar to a watchdog, but the chosen periodicity is a hard deadline and cannot be extended by the controlled processor boards.
Single event upsets can have different effects depending on the data they are affecting. If the memory contains raw data coming from sensors used for housekeeping or for simple monitoring, they are probably leading only to the invalidation of one or some of these data: the overall system behavior is not changed. But, if the memory involved is containing operating code or parameters used for system configurations, we can have a misbehavior in the operations executed by our satellite, eventually causing damages. Obviously the latter are more troublesome and have to be avoided in all the possible ways.
In particular, the FeRAM device contains some functional parameter and not only housekeeping data, therefore we had to make an extra effort in ensuring the memory tolerance to the harsh environment. As we exposed earlier in this chapter even if the FeRAM memory cell can resist to higher cosmic radiation levels than other technologies, the presence of CMOS elements in the boundary circuitry can cause changes in the stored data (SEFI). The solution we chose was to reduce the power on time, in order to reduce the time window where the memory is sensitive to radiation effects and to replicate in three different portions of the device the functional parameters. Replication of telemetry was not deemed vital and not performed.

7.5.3 Power considerations

PiCPoT is a portable system, even if unconventional. Indeed it is a battery based system and even if it is also powered by solar panels, it has to survive during the Sun eclipse periods (about 40 min per 90 min orbit), thus every part of the system should be optimized for power, as in all the portable devices we deal with everyday.
In Tab. 2 we can see the power budget for each subsystem and in particular for the on-board processors. This small amount of energy available has to be used effectively in all the processor boards, i.e., microcontrollers, analog conditioning, and memories.
In our case the external memory is used for two main purposes:

Configuration The OBC can be configured to select different available choices, thus at the beginning of each power cycle, the processor reads from the outer memory which configurations have been set and reacts accordingly. Typically these selections are changed only during the system programming, or by asking from ground to reconfigure the system in case of damages. Thus, the locations containing such information are mainly read.

Storage of telemetry data When we activate the OBC it acquires all the values of all the sensors available and reads all the event counters, in order to build a snapshot of telemetry data. After completion, telemetry is stored in the external memory, together with running statistics of all the parameters. These data are read when they have to be transmitted to ground. This usage is more focused on both reading and writing operations.

FeRAM devices have the advantage of being more power efficient in writing operations. Since we are accessing this memory in a balanced way for reading and writing, the usage of FeRAM devices helped us in reducing the amount of power required for writing operations. Moreover, being able of completing a writing operation in few tens of nano seconds, instead of tens of milliseconds (as in case of Flash devices), they allow further power saving, since the system can suspend earlier its operation.

Device	Duty Cycle	Peak Power	Avg Power
PowerSwitch	100%	20 mW	20 mW
Proc A & B	6%	200 mW	12 mW
Payload	0.5%	3.84 W	21 mW
TxRx	2.6%	17.2 W	443 mW
Losses in Batteries & switching			1.07 W
Solar Panels			-2.24 W
Margin			-674 mW

Table 2. Power budget

7.5.4 Project remarks

Unfortunately we were not able to test this design in space since the launcher blew up during the launch, causing the destruction of 14 nano-satellites (Malik (2006)). It has been a shame, since operational data from the design in the environment it has been designed for, would have produced a great feed-back on our design techniques and solutions. Luckily the grown experience has been reused in the new project we are working on, that is described in the next section.

7.6 A modular architecture for nano-satellites

Thanks to the experience got by the design of PiCPoT we decided to use again FeRAM devices in our new spaceborne project, called AraMiS, presented in Speretta et al. (2007). The aim of this project is to design, prototype and develop a new architecture for modular small satellites. The most effective way to reduce the cost of a nano- or micro-satellite mission is to reduce as much as possible design and non-recurrent fabrication costs, which usually account for more than 90% of the overall budget. Reducing them can be achieved only by sharing the design among a large number of missions.

Design reuse is the rationale behind the AraMiS project, that is to have a modular architecture based on a small number of flexible and powerful modules which can be reused as much as possible in different missions. Using the same module(s) more times obviously allows to share design, qualification and testing costs and to reduce the time-to-launch.

The first step in the AraMiS project has been to identify the most common and critical subsystems. We have then concentrated our efforts on the following subsystems, which are described in details in Speretta et al. (2007) and in Speretta et al. (2009):

1. mechanical subsystem;
2. power management subsystem;
3. telecommunication subsystem;
4. on-board processing subsystem;
5. payload support.

The basic architecture of AraMiS is based on one or more modular *intelligent tiles*. Most of them are to be regularly placed on the outer surface of the satellite and have a double function: *mechanical* and *functional*. The inner part of the satellite is mostly left empty (except for the on-board processor and payload support tile), to be filled by the user-defined payload, which is the only part to be designed and manufactured ad-hoc for each mission.

The *power management* subsystem aims at managing all the aspects related to energy, i.e., collecting energy from solar cells, storing it on the available batteries, and guaranteeing their correct discharge when modules requires energy to operate. The *telecommunication* subsystem

contains the modems, the transceivers, the radio-frequency components, and the antennas used to communicate with the ground stations. The *on-board processing* subsystem contains the main processors and units devoted to the computation and the high speed communication among the tiles and the modems. At last, the *payload* subsystem is the only part not designed at the moment, since it can vary from mission to mission, thus we only developed the communication and the mechanical interfaces.
Each tile is designed, manufactured and tested in relatively large quantities. Reuse also allows to put an increased design effort to compensate for the lower reliability of COTS devices, therefore achieving a reasonable system reliability at a reduced cost.

7.6.1 Modularity and customization

The aim of our design is to study, develop, and produce a structure, a set of tiles, and a set of interfaces to allow universities and small enterprise to access the space in a easy and affordable way.
Thus the concept of modularity in all part of our design has to be the *leit motif*. Modularity means a set of redundant functions and resources that can be configured and used when needed (both during the pre-launch phase and at run-time). Many of these features have to be changed easily, thus using a configuration memory is the straightforward choice. The number of available selections is pretty limited (i.e., can vary from 10 to hundred in the projects we have foreseen), but they have to be maintained for all the satellite life. For this reasons FeRAM devices are the most suitable to this goal.

7.6.2 Operational conditions

The target environment for our design is again the low-earth orbit, a zone between the 500 km and the 800 km above the sea level. The environment is the same of the PiCPoT satellite we described above, thus the related constraints are the same.

7.6.3 OBC-tile architecture

The OBC-tile architecture is shown in Fig. 6. It is based on a hot redundancy structure relying on FPGAs and CPUs. This OBC relies on the presence of an MSP430 (TI (2010)) microcontroller and an Actel FPGA A3P125. The former is used for handling basic operation of the tile, like the communication through the control bus, sensors acquisition, JTAG interface... The latter is aimed at performing all the *data crunching* related to the image elaboration and the high speed communication with the payload and the radio subsystem.
In order to save power the FPGA is switched on only when needed and the MSP430 is enrolled to manage the power cycling of this device.
Since this module has to be able to work in different cases (e.g., different power cycles, different hardware configurations, different payloads, ...) we need to keep trace of all these choices somewhere. Obviously a memory is a good place to keep it, but due to our power constraints, we need to shut the memory down when it is not accessed. Thus the usage of a non-volatile technology is mandatory and, how we exposed before for the PiCPoT case, FeRAMs is the best choice.
In our case we use multiple smaller chips, even if greater ones are commercially available, for reliability reasons, since in case of physical damages we can have multiple places where to save our configuration data. Moreover having multiple chips allows us to save more energy since we power only the device needed, and not all the memory we have on board.

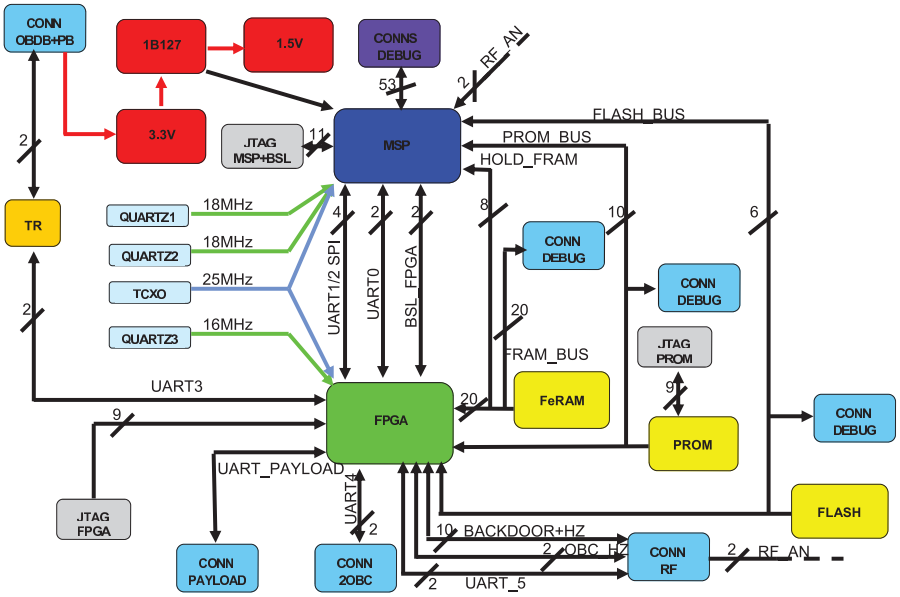

Fig. 6. AraMiS OBC architecture

8. Conclusions

This chapter has shown how commercial-off-the-shelf FeRAM devices can be a good solution for spacecrafts. Indeed we described how the FeRAM memory cell is far less sensitive to the issues we can have in space (i.e., heavy ions and total ionizing dose). Moreover its intrinsic low power consumption allow the devices to be very well suited for battery-based devices and those applications where heat dissipation is difficult.

After this introduction two real designs have been presented, where the usage of FeRAM memories has produced a set of non negligible improvements. Further investigations are ongoing and we plan to use again these devices in our future projects, in order to make our designs safer and more reliable.

Unfortunately we did not collect data from the PiCPoT experiment, since it blew up during the launch due to a failure of the launcher. But the new project will provide us a lot of information from the real application field allowing us to increase our expertise in using these kind of devices in the space and will allow our future designs to be more reliable, robust, and efficient.

9. References

Benedetto, J., Derbenwick, G. & Cuchiaro, J. (1999). Single event upset immunity of strontium bismuth tantalate ferroelectric memories, *Nuclear Science, IEEE Transactions on* 46(6): 1421 –1426.

Gray, P. R., Hurst, P. J., Lewis, S. H. & Meyer, R. G. (2001). *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Inc.

Kamp, D., DeVilbiss, A., Haag, G., Russell, K. & Derbenwick, G. (2005). High density radiation hardened ferams on a 130 nm cmos/fram process, *Non-Volatile Memory Technology Symposium, 2005*, pp. 4 pp. –51.

Malik, T. (2006). Report: Dnepr rocket crashes shortly after launch.
URL: *http://www.space.com/2669-report-dnepr-rocket-crashes-shortly-launch.html*

Miyahira, T. & Swift, G. (1998). Evaluation of radiation effects in flash memories, *Proceedings of the Military and Aerospace Applications of Programmable Devices and Technologies Conference*.

NASA-Gsfc (2000). *Single Event Effects*.
URL: *http://radhome.gsfc.nasa.gov/radhome/see.htm*

Nguyen, D. N. & Scheick, L. Z. (2001). TID testing of ferroelectric nonvolatile RAM, *Proceedings of the Radiation Effects Data Workshop*, Vancouver, BC, Canada, pp. 57–61.

Passerone, C., Tranchero, M., Speretta, S., Reyneri, L. M., Sansoè, C. & Del Corso, D. (2008). Design solutions for a university nano-satellite, *Proceedings of the Aeroconf*.

Philpy, S., Kamp, D. & Derbenwick, G. (2003). Hardened by design ferroelectric memories for space applications, *Non-Volatile Memory Technology Symposium, 2003*, p. 4 pp.

Scheick, L., Guertin, S. & Nguyen, D. (2004). *SEU evaluation of FeRAM memories for space applications*.
URL: *http://klabs.org/richcontent/MemoryContent/nvmt_symp/nvmts_2002/docs/21/21_scheick_p.pdf*

Sheikholeslami, A. & Gulak, P. (2000). A survey of circuit innovations in ferroelectric random-access memories, *Proceedings of the IEEE* 88(5): 667 –689.

Shiga, H., Takashima, D., Shiratake, S., Hoya, K., Miyakawa, T., Ogiwara, R., Fukuda, R., Takizawa, R., Hatsuda, K., Matsuoka, F., Nagadomi, Y., Hashimoto, D., Nishimura, H., Hioka, T., Doumae, S., Shimizu, S., Kawano, M., Taguchi, T., Watanabe, Y., Fujii, S., Ozaki, T., Kanaya, H., Kumura, Y., Shimojo, Y., Yamada, Y., Minami, Y., Shuto, S., Yamakawa, K., Yamazaki, S., Kunishima, I., Hamamoto, T., Nitayama, A. & Furuyama, T. (2010). A 1.6 gb/s ddr2 128 mb chain feram with scalable octal bitline and sensing schemes, *Solid-State Circuits, IEEE Journal of* 45(1): 142 –152.

Shooman, M. (2001). *Reliability of Computer Systems and Networks*, John Wiley & Sons, Inc.

SPENVIS (n.d.). *SPENVIS, the Space Environment Information System*.
URL: *http://www.spenvis.oma.be/*

Speretta, S., Reyneri, L. M., Sansoè, C., Tranchero, M., Passerone, C. & Del Corso, D. (2009). Optical-based cots data communication bus for satellites, *Acta Astronautica* 66: 674–681.

Speretta, S., Reyneri, L., Sansoè, C., Tranchero, M., Passerone, C. & Del Corso, D. (2007). Modular architecture for satellites, *Proceedings of 58th International Astronautical Congress*, Hyderabad, India.

TI (2010). *MSP430 Family User's Guide*.

Ziegler, J. F., Curtis, H. W., Muhlfeld, H. P., Montrose, C. J., Chin, B., Nicewicz, M., Russell, C. A., Wang, W. Y., Freeman, L. B., Hosier, P., LaFave, L. E., Walsh, J. L., Orro, J. M., Unger, G. J., Ross, J. M., O'Gorman, T. J., Messina, B., Sullivan, T. D., Sykes, A. J., Yourke, H., Enger, T. A., Tolat, V., Scott, T. S., Taber, A. H., Sussman, R. J., Klein, W. A. & Wahausand, C. W. (1996). Ibm experiments in soft fails in computer electronics, *IBM Journal of Research and Development* 40(1).

11

Adaptive Boolean Logic Using Ferroelectrics Capacitors as Basic Units of Artificial Neurons

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1. Introduction

Neural networks are being investigated as a computational paradigm in many fields of artificial intelligence.

The pioneers of cybernetics were clearly inspired by neurology and the current knowledge of the human brain to develop the architectures of modern computing machines. The evolution has given the brain very distinctive capabilities of learning, distributed memory, computation, generalization, robustness, and the capability of interpretation of imprecise and noisy information, etc., not present in Von Neumann computers.

Neuroengineers have come up with the idea of using Artificial Neural Networks (ANNs) massively parallel computing machines inspired by the biological nervous systems. However, ANNs have a very different approach and computing paradigm, where learning from examples and learning from iteration replaces our common idea of programming. These models achieve good performance via massively parallel networks composed of generally nonlinear computational elements, referred to artificial *neurons*. Synaptic weights are associated with each neuron connection between neurons. In the case of classical ANNs, the activation potential and the synaptic weights are analogous, respectively, to the firing rates and the strength of the synapse in biological neurons which are arranged in layers.

The first, very simplified model, mathematical model of a neuron operating in an all-or-none fashion: the Threshold Logic Gate (TLG). It did not take very long for a hardware implementation to be developed. Since then a lot of researh have been developed with the aim of implementing artificial neurons in hardware and construct intelligent systems On-Chip.

Many theoretical results have been shown that threshold logic circuits are more powerful and/or efficient than Boolean circuits (Beiu et al., 2006). Exploiting the principle for electronics circuits may reduce the number of transistors and interconnections (Shibata and Ohmi, 1991). Output-wired threshold gates working in the classical above threshold domain have been implemented, too. A lot of work has been done in this area. Thinking on this scenario, this chapter shows a implementation of the boolean logic with artificial neuron type model with a

Ferroelectric (Fe) capacitor as its basic unit. The Fe Capacitors was chosen because it have been embedded into LSIs as Ferroelectric Random Access Memory (FeRAM) and their reliability data have been accumulated. The capacitors are high impedance device, and it is an advantage for low power consumption, besides the configuration can be changed after packaging. The FeCapacitor uses the phenomenon of the hysteresis loop as the activation function for the neuron model. The model performs a weighted sum of the inputs and applies it the non-linear activation function generated by a single side of the hysteresis. Changing the weights, it is possible to reconfigure the gate easily. Ones tries to show a new way of implementing a neuron, without using transistors.
We developed the perceptron model with the FeCapacitor, that we called here FePerceptron, and we also developed the FeSpiking Neuron model, that is an extended model for the spiking neuron (Guerreiro et al., 2008) using the FeCapacitor as its basic unit for the activation function. Both models is going to be simulated and tested in Matlab. The models were used to simulated all logical gates and synthesis of several digital circuits as D-flip-flop, shif-register, full adders, and a simple CPU with the Spiking FeNeuron. The Spiking FeNeuron is developed because it can simulated all logical gates, inclusive the XOR gate with single neuron, which is impossible with a single Perceptron.
Because of the simplicity, we started the hardware implementation with the FePerceptron in an Field Programmable Gate Arrays (FPGA). The FeCapacitor is developed as its basic unit and can be used in any neuron model as activation function. We used the DSP builder of Altera to generate the model. The DSP Builder Signal Compiler block reads Simulink Model Files developed (.mdl) that are built using DSP Builder blocks and generates the VHDL files. This is the first step of a work to implement in hardware the neuron using FPGAs simulating the desired hardware, bringing a second degree of reconfigurability to the FPGAs with the adaptive boolean logic CPU.
This chapter is organized as follow, first in section 2 we give an overview of several developed works and researches that were done simulating and implementing neural networks in hardware. Section 3 shows the development of the mathematical model of the FeCapacitor. The FeCapacitor model is used as activation function to the Perceptron model generating the FePerceptron and to the Extended Spiking Neuron model generating the FeSpiking Neuron Model as shown in section 4. The simulations in Matlab of both models are shown in section 5 with the realization of boolean logic gates and adaptive boolean circuits. The section 6 is responsible to shown the FePerceptron model developed in an FPGA. Finally, conclusion are presented in section 7.

2. History of neuron models, simulations and implementation of neural networks in hardware

The hardware implementations means and introduces for example computational errors, degradation of learning and lack of accuracy in results. This are some issues that have been studied and address and explored in many researches. These include digital (Bermak and Martinez, 2003; Kung, 1992; Lenne, 1995), analog (Brown et al., 2004; Mead, 1989), hybrid (Lehman et al., 1996; Schmid et al., 2004), FPGA based (Nedjah and Mourelle, 2007; Rak et al., 2009; Schrauwen and D'Haene, 2005), and (non-electronic) optical implementations (Moerland, 2007; Tokes et al., 2000).
In spite of all the difficults to implement ANN in hardware a lot of research have been done. There is a lot of needs in real-world applications. Some examples are: optical character recognition, robotics, voice recognition, adaptive filters, image analysis, finger print feature

extration, acoustic sound recognition, olfactory sensing, traffic monitoring, experiments in high energy physics (Lamela and Ruiz-Llata, 2005), and adaptive control.
There are indeed several surveys which have appeared in the past. There is this one (Janardan and Indranil, 2010) that has done a survey which includes most of all works concerning Hardware Neural Networks (HNN). Here, we only give a small overview over what was done in the past based on (Janardan and Indranil, 2010), so the importance of the HNN can be noticed, and seen that a lot of research has already been developed. Some early references on the VLSI implementations can be found on (Mead, 1989) and (Glesner and Poechmueller, 1994). An overview on neurocomputers up to the 90's, built from accelators boards, general purpose hardware, and neurochips can be found on (Heemskerk, 1995). Digital implementations with custom processors can be found (Ienne, 1996).
Sundararajan and Saratchandran (1998) discuss in detail various parallel implementation aspects of several ANN models using various hardware architectures. Zhu and Sutton (2005) survey FPGA based implementations of ANNs discussing different implementation techniques and design issues. Smith also discuss and survey digital and analog VLSI implementations approaches in neural model.
One of the latest surveys with specific focus to commercially available hardware can be found on Dias et al. (2004). Neurofuzzy hardware systems is discussed concerning aspects of various tecnologies of hardware implementations and software co-design techniques. Implementations of Spiking Neural Networks is provided by (Schrauwen and D'Haene, 2005). Valle (2005) presents various approaches to built smart adaptive devices.
There still some topics as hardware friendly learning algorithms, as pertubation learning (Jabri and Flower, 1991), constructive learning (Smieja, 1993), cascade error projection learning (Duong, 1995; Duong and Stubberud, 1995), and local learning (Chen et al., 2000). Some HNN based on Multilayer Perceptron (MLP) (D'Acierno, 2000; Kumar et al., 1994), radial basis function (Fakhraie et al., 1994; Verleysen et al., 1994; Yang and Paindavoine, 2005), and Neocognition (Patnaik and Rao, 2000) and neurocomputers(Glesner and Poechmueller, 1994; Strey and Avellana, 2000).

3. The mathematical model of ferroelectrics capacitor

There are two areas of research to be investigate, the physically based models and the behavioral models. In our work, the bahavioral modeling was chosen because it does not required a detailed knowledge of ferroelectric theory; it only requires a careful observation of the ferroelectric capacitor behavior from the circuit point of view.
A lot of research have been done in attempts to models the behavior of a ferroelectric capacitors (for a review, see: (Sheikholeslami and Gulak, 1997) since they were introduced as storage elements in integrated nonvolatile memory applications.
In this paper, the Mathematical Model (Miller et al., 1991) is used that introduces a closed form mathematical equation for the hysteresis loop.
Based on the saturability of the switching polarization and the symmetry of the hysteresis loop, the mathematical model approximates the saturated polarization loop with two hyperbolic functions:

$$P_{sat}^{+}(E) = P_s tanh[\frac{E - E_c}{2\delta}] \tag{1}$$

and,

$$P_{sat}^{-}(E) = -P_{sat}^{+}(-E) \tag{2}$$

where $P_{sat}^{+}(E)$ and $P_{sat}^{-}(E)$ represent the polarization corresponding to the positive and negative going branches of the hysteresis loop, respectively. P_s and E_c are the saturation polarization and the coercive field extracted from an actual hysteresis loop. With the fixed P_s and E_c, δ is uniquely specified by P_r, the remanent polarization, through the following equation:

$$\delta = E_c[ln(\frac{1 + P_r/P_s}{1 - P_r/P_s})]^{-1} \tag{3}$$

A sketch of the hysteresis loop is done with MATLAB as it is shown in Figure 1. The symmetry with respect to the origin in this Figure is guaranteed by Equation (2).

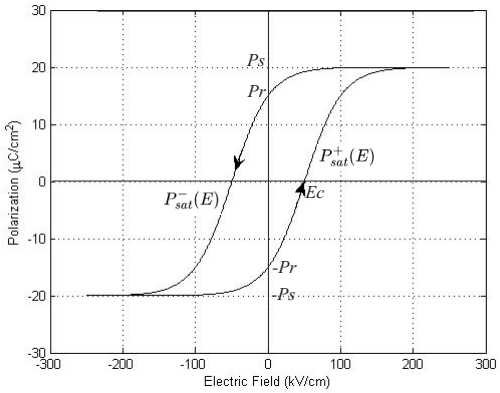


Fig. 1. The hyperbolic tangent functions approximate the Saturated Polarization Loop. The hysteresis loop is plotted considering the values of $P_s = 23\ \mu\ C/cm^2$, $P_r = 15\mu\ C/cm^2$, and $E_c = 40\text{kV}/cm^2$ borrowed from an actual saturated hysteresis loop.

The Mathematical Model provides a good approach for steady-state analysis of ferroelectric capacitor behavior, and this model is sufficient by now for this work. Future simulations maybe can incorporate the transient analysis and by than mode accurate models can be necessary.

4. The ferroelectrics capacitor as an activation function of artificial neurons

4.1 Perceptron model

The biological neuron is the structure unit of the nervous systems. It considers of a cell body, called soma, axon and several ramifications. These ramifications are called, dendrites. The dendrites conduct action potentials or electrical pulses toward the body cell and conform in large and complicated trees. The dendrites and the soma constitute the input surface of the neuron. The axon consists of a large fiber whose branches form the axonal tree. The axon has a arborization at its terminal. The tips of the branches of the axon are called nerve terminals, boutons or synaptic knobs. The axon acts as a transmission line. The action potential travels along an axonal tree all the way to the nerve terminals. The terminals of the branches make contacts with the dendrites of other neurons. The contacts are called synapses.

The first computational model of the biological neuron was introduced by McCulloch and Pitts (McCulloch and Pitts, 1943) in the 1940s. McCulloch and Pitts merged mathematical logic and neurophysiology to propose a binary threshold unit as a computational model for an artificial neuron operating in discrete time. The output $y_k(t)$ of a neuron is 1 when an action potential is generated, and -1 otherwise. A neuron fires when the effects of inhibitions and excitations are larger than a certain threshold, θ.
In 1958, the American psychologist Rosenblatt proposed a computational model of neurons that he called *The Perceptron* (Rosemblatt, 1958). The essential innovation was the introduction of numerical interconnection weights.
A neuron is an information processing unit that is fundamental to the operation of a neural network (Haykin, 1998). The perceptron model of the neuron has three basic elements (Figure 2):

1. Synapses that are characterized by the strength of the weights;
2. An adder for summing the input signals, weighted by the respective synapses and the threshold of the neuron;
3. An activation function for limiting the amplitude of the output (in this case completely unclocked with the firing event).

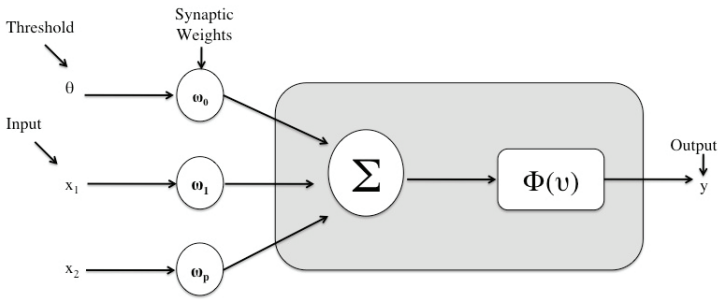


Fig. 2. Perceptron Model

The external threshold, denoted by θ, has the effect of increasing or lowering the net input of the activation function, depending on whether it is positive or negative.
The perceptron consists of a linear combiner followed by a non-linear function, as depicted in Figure 2. The summing node of the neuronal model computes a linear combination of the inputs, x_i, applied to the synapses connections, w_i, and also incorporates an external threshold, θ. The resulting sum, that is, the induced local field, is applied the activation function. The activation function denoted by $\Phi(v)$, defines the output of the neuron in terms of the local field, v. The activation function usually used is a sigmoid. The weights model the synaptic strength, and the output of the neuron models the rate of fire of biological neurons. The threshold can be accounted for in two ways: adding a new input signal fixed at $+1$ or adding the threshold to the linear combination of the input with the weights.
The neuron can be described mathematically as:

$$v = \sum_{j=1}^{p} \omega_j x_j \tag{4}$$

and

$$y = \phi(v + \omega_0\theta) \tag{5}$$

The capacity of learning is one of the most important characteristics of an ANN. Learning is closely related to an improvement of performance of the system. This is achieved by minimizing errors, self-organizing information through correlations of data, and maximizing rewards in a trial-and-error system over time. In practice, learning is achieved by adjustment of the free parameters of the ANN.

4.1.1 The FePerceptron model

Our simplified model is based on the perceptron model, using the following concepts: inputs, synapses strength, adder, activation function and the threshold.
The FeNeuron uses the ferroelectric capacitor as its basic unit. The model (Figure 3) is composed by the input, x_i, by the synaptic weights, w_i, as resistors, combining them linearly. The result is applied to the ferroelectric capacitor performing the output of the model. The phenomenon of the hysteresis loop is used to act as the activation function. It is necessary to use only one side of the hysteresis loop.

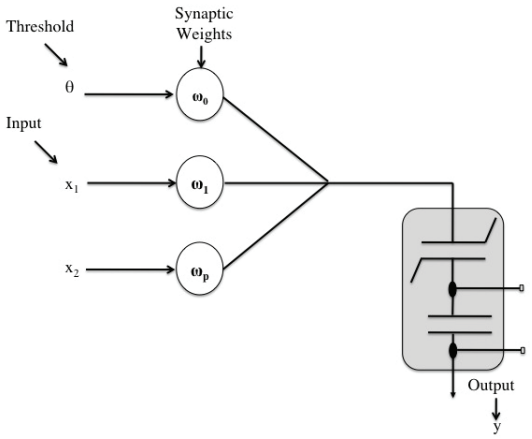


Fig. 3. The FeNeuron Model

The induced local field of the neuron is computed as in Equation (4). The output is described as:

$$y = P^{+}_{sat}(v + \omega_0\theta) \tag{6}$$

and,

$$P^{+}_{sat} = P^{+}_{sat}/P_s \tag{7}$$

The Equation (6) can be re-written as:

$$y = P^{+}_{sat}(\sum_{j=1}^{p} \omega_j x_j + \theta) \tag{8}$$

The goal of the model in this case is to classify correctly the set of externally applied stimuli, $x_1, x_2, x_3, ..., x_p$ into two classes. In our work, we are treating with Boolean functions with

two inputs, thus our network is a single layer, with only one neuron with two inputs plus the threshold and one output.

4.2 Extended Spiking Neuron model

Artificial spiking neurons are biophysical models which try to account for properties of biological neurons by modeling the integrated signal flow through parts of the neuron. The input spike signals, from presynaptic biological neurons are weighted, summed up and passed through a type of leaky integrator. If the membrane potential exceeds a certain threshold, a spike is generated. The pulses arrive at the input synapses in discrete time. The Extended Spiking FeNeuron is a discrete model composed of an input layer, synaps weights, first order recursive filters, a soma, a hard limiter and the membrane potential. The input layer receives the input spikes. The weights are the synaptic strength values. The soma provides a linear combination of the input signal passing through the first order recursive filters and summing with the thresholds coming from the feedback loop. The hard limiter compares the soma potential with the threshold and emits a spike depending on the soma threshold.
The membrane potential is responsible to compute the delay necessary for the neuron to compute. The delay is build up by the summing potential of the input signals and depends on the time delay of the filters and more important on the delay caused by the feedback loop where the dynamic threshold sets the time of firing. We can define a neuron i that receives inputs from presynaptic neurons $j \in \Gamma_j$, where

$$\Gamma_i = \{j/j \ \ presynaptic \ \ to \ \ i\} \tag{9}$$

The discrete model considers a "1" for a incoming spike and "0" for the absence of a spike. The input passes through the first order recursive filters and then is summed up. The Equation 10 describes the action of the first order recursive filters:

$$u_{fij} = e^{-(T/\tau_{ij})} u_{fij}(n-1) + \omega_{ij}(n) x_{ij}(n) \tag{10}$$

where $x_{ij}(n)$ is the input of the synapses, $w_{ij}(n)$ is the synapses weight, T_{ij} is a constant delay of the filter, $u_{fij}(n)$ is the output of the first order recursive filter in a time slice, n.
The dynamic threshold is describe by the following equation:

$$\theta(n) = \vartheta + \theta_1(n) \tag{11}$$

$$\theta_1(n) = p_i(n) r_i(n) \tag{12}$$

where ϑ is the static threshold and $pi(n)$ is the output of the first order recursive filter of the feedback loop.
The r(n) is defined as:

$$r_i(n) = \xi(|p_i(n)| - \sum_{j=1}^{q} x_{ij}(n)) \tag{13}$$

where q is the length of the input vector.
The function $\xi(.)$ is defined as:

$$\xi(v) = 1/2 + 1/2(erf(v/(2k))) \tag{14}$$

This function is implemented by the Ferroelectric Capacitor.

The equation of the first order recursive filter of the feedback loop is:

$$p_i(n) = ap_i(n-1) + g_i(n) \tag{15}$$

where $g_i(n)$ is the output dependent on $y_i(n)$ and $r_i(n)$

$$g_i(n) = \xi(r_i(n) - y_i(n)) \tag{16}$$

The state $mp_i(n)$ of the model neuron i can be rewritten as:

$$mp_i(n) = -\{v + p_i(n)r_i(n)\} + \sum_{j\in\tau}(\omega_{ij}(n)u_{fij}(n)) \tag{17}$$

The output $y_i(n)$:

$$y_i(n) = \xi(mp_i(n)) \tag{18}$$

The process of accumulation voltage and transformation to time is described by the block diagram named as membrane potential in Figure 4. From the figure we notice that $\theta_1(n)$ depends on the feedback of the output and on the input signals. The filter of the feedback loop is a first order recursive filter with the coeficient equal to a. The absolute value of the filter output $(pi(n))$ subtracts from the sum of the inputs. Until the filter output reaches the sum of the inputs, the feedback loop accumulates voltage. This is done, by passing the response of $|p_i(n) - \sum_{j=1}^{q} x_{ij}(n)|$ through the $\xi(v)$ function (Eq. 7), resulting in $r_i(n)$. The $\xi(v)$ function is implemented by hystheresis of the FeCapacitor. The result of $r_i(n)$ is equal to 1 when the output of the filter is equal or greater to the sum of the input signal, and 0 otherwise. The $r_i(n)$ is multiplied by $(p_i(n))$ resulting in the dynamic threshold that is the response of the membrane po- tential block diagram. The dynamic threshold accumulates charge until a spike occurs and the filters are reset. Our work has mapped the biological behavior of accumulating charge to create the receptor field by adding the membrane potential block diagram described in Figure 4 to the spiking neuron model. Using this approach it is possible to solve non-linear problems (XOR - problem) with a single neuron with the hard limiter function as activation function $(\xi(v))$.

5. The simulations of the models in simulink by Matlab

5.1 FePerceptron model

The results show the the simulation of the FeNeuron performing the logic gates, AND, OR, NAND and NOR. The model performs thresholding operations with a very simple architecture. It was developed in MATLAB environment.

The simulated gates have an architecture of a single neuron. The synaptic weights, ω_1 and ω_2 of the model were adapted iteration-by-iteration basis. For the adaptation process, the neuron was trained with the error-correction rule as a convergence algorithm. This algorithm uses a supervised paradigm which means that the desired response is presented in the training process. The desired response is the output of the logic gate that has been simulated with the respective input, following the well-known truth table of logic gates.

The algorithm can be described as follow:

Variables and Parameters:

The inputs: $\mathbf{x}(n) = [\theta \;\; x_1 \;\; x_2]^T$

The weights: $\mathbf{w}(n) = [\omega_0 \;\; \omega_1 \;\; \omega_2]^T$

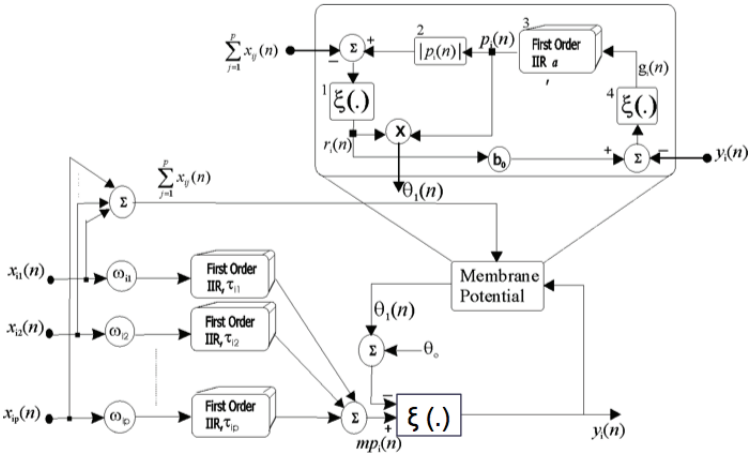


Fig. 4. The Discrete Spiking FeNeuron Model

The actual response: $y(n)$
The desired response: $d(n)$
The learning rate, or a positive constant less than a unit: η
The mean square error: $error(n)$

1. Initialization: Randomize $\mathbf{w}(n)$. Perform the computations from $n = 0, 1, 2, ...$ until the mean square error is minimum.
2. Computation of the actual response with (18).
3. Adaptation Process:

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \eta[e(n)]\mathbf{x}(n) \tag{19}$$

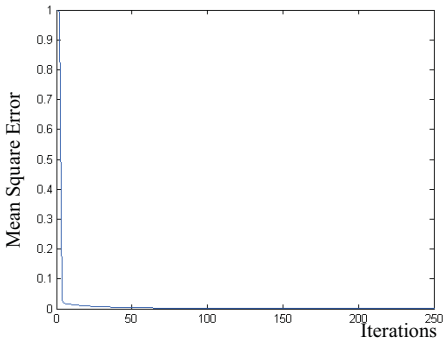
$$e(n) = d(n) - y(n) \tag{20}$$

$$error(n) = \frac{1}{2}\sum_{j\in\Gamma} e^2(n) \tag{21}$$

   where Γ includes all neurons in the output layer of the network. In our case, only a single neuron is used.

4. Increment time step n by one and goes back to 2.

After the training process, the weights were computed and can be used to simulate the logic gates. The learning curves are shown in Figure 5 with the computed parameters.
The model performs thresholding operations with a very simple architecture. The Boolean functions performed by the model is soft programmable. This is accomplished by only adjusting the weight values of the synaptic connections. It is a very simple model that was easily implemented by software and can be extended to hardware implementations. As hardware implementations, this model brings the contribution of being very simple and can perform several functions with only changing the free parameters of the structure that can be soft-programmable.



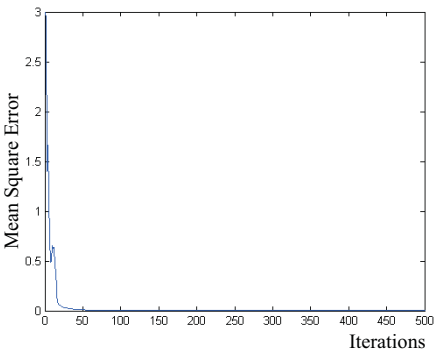
AND GATE

Weights = [-0.3759 0.6389 0.6389]

Actual Output = [-0.0006 0.0015 0.0015 0.9981]

Desired Output = [0 0 0 1]

Minimum error = 0.0000059874



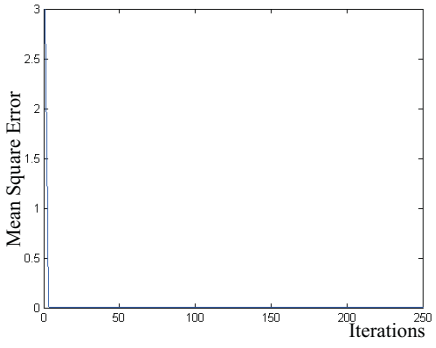
NAND GATE

Weights = [1.5709 -0.6503 -0.6503]

Actual Output = [1.0000 0.9988 0.9988 0.0017]

Desired Output = [1 1 1 0]

Minimum error = 0.0000059874



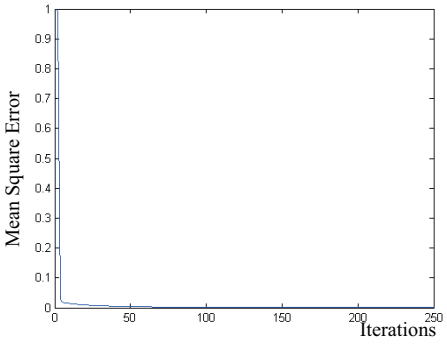
OR GATE

Weights = [0.2528 0.7089 0.7089]

Actual Output = [0.0013 0.9995 0.9995 1.0000]

Desired Output = [0 1 1 1]

Minimum error = 0.0000020539



NOR GATE

Weights = [0.9145 -0.6688 -0.6688]

Actual Output = [0.9986 0.0011 0.0011 -0.0009]

Desired Output = [1 0 0 0]

Minimum error = 0.0000052702

Fig. 5. The learning curves with the parameters for each computed logic gate. The inputs were (0 0), (0 1), (1 0) and (1 1). The threshold was considered equal to +1 for all gates.

5.2 Spiking FeNeuron model

In a digital simulation, the time period, n, is called a time slice. The four major steps of computing are:

1. Input phase: The input of each synaptic dendrite connection multiplied with the respective synaptic weight.

$$\alpha_{ij}(n) = \omega_{ij}(n)x_{ij}(n) \tag{22}$$

2. Filter phase: The signals from the input phase pass through the recursive filters.

$$ufij(n) = \alpha_{ij}(n) + e^{-\frac{T}{\tau_{ij}}} u_{fij}(n) \tag{23}$$

3. Output phase: The sum of the signals from the filter phase are summed to produce the membrane potential. If the membrane potential exceeds the dynamical threshold, an output spike is generated.

The state $mp_i(n)$ of the model neuron i can be rewritten as:

$$mp_i(n) = -\{v + p_i(n)r_i(n)\} + \sum_{j\in\tau}(\omega_{ij}(n)u_{fij}(n)) \tag{24}$$

$$p_i(n) = ap_i(n-1) + g_i(n) \tag{25}$$

$$g_i(n) = \xi(r_i(n) - y_i(n)) \tag{26}$$

$$y_i(n) = \xi(mp_i(n)) \tag{27}$$

$$\xi(v) = \frac{1}{2} + \frac{1}{2}erf(\frac{v}{2k}) \tag{28}$$

If the spike is generated, the filters are reset. Otherwise the filter still accumu- lates potential.

4. Learning phase: The synaptic weights are adjusted with the Steepest Descent method.

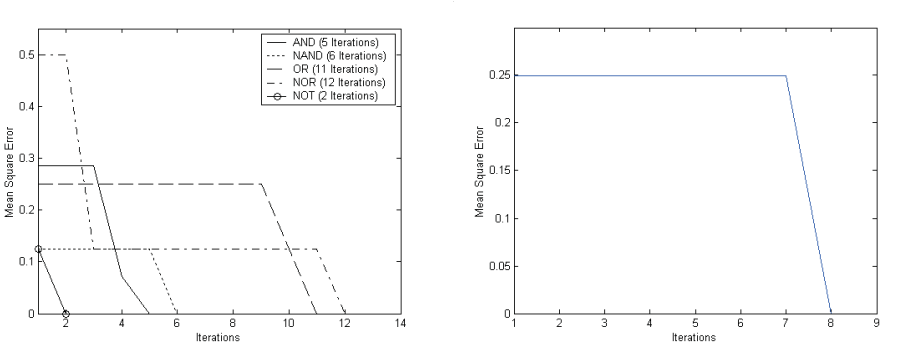
$$\omega_{ij}(n+1) = \omega_{ij}(n) + \gamma(d_i(n) - y_i(n))x_{ij}(n) \tag{29}$$

where $d_i(n)$ is the desired output, $y_i(n)$ is the actual output, $x_{ij}(n)$ is the input, and γ is the learning rate.

These computation steps will be used in the logical functions problems. The computation of Boolean functions is a classification problem and as such it consists of separating the data into classes based on a discriminant function. There are two classes (0 or 1), and the input space is composed of four entries, each one with length two, except for the NOT logical gate that has one input and one output that negates the input.

Figure 6 (a) shows the learning curve for all logical gates and Figure 6 (b) shows for the XOR. The training phase is the same for all Boolean functions, we just have to modify the desired output to suit each logical gate. The weights and the filter coeficient are summarized in table I. The learning rate used was 0.01 and the filter coeficients of the first order recursive filter (τ_{ij}) were 0.01. Depending on the learning rate and the initial values of the weights the convergence rate changes.

Figure 7 shows the new symbol adopted for the neural logical gates and the output vector after the training process. The result is a perfect truth table of the respective logical gates. Table 1 shows the values for the decay constants, the weights and the learning rates for each logical



(a) The logical gates learning curves. (b) The XOR logical gate learning curves.

Fig. 6. Learning curves.

gate. The Spiking FeNeuron model is composed by the input, $x_i(n)$, by the synaptic weights, $\omega_i(n)$, passing by the RC filters. The result is applied to the ferroelectric capacitor ($\xi(.)$) performing the output of the model. The phenomenon of the hysteresis loop is used to act as the the activation function. Using one side of the hysteresis that can be easily simulated as an error function. The simplicity of the Integrate-and Fire (IF) model is a good advantage. Others models, as quadratic IF, IF with adaptation, integrate- and-fire-or-burst and resonate-and-fire are extension and improvement of the integrate-and-fire model. These models are worried in capture the firing dynamics of real neurons (Janardan and Indranil, 2010). The main focus of this work is to generate a model that is able to compute and to be applied in engineering problems with a single neuron model and later with a network of neurons.

Parameters	AND	NAND	OR	NOT	XOR
Weights (ω_{ij})	0.48/0.48	-0.39/0.69	0.98/0.88	0/-1	0.568/-0.255
Decay constants (τ_{ij})	0.01/0.01	0.01/0.01	0.01/0.01	0.01/0.01	0.01/0.01
Learning rate (γ)	0.01	0.01	0.01	0.01	0.01

Table 1. Parameters of the Spiking FeNeuron.

5.3 Realization of the adaptive logic circuits

In this work the boolean logical gates are simulated by the Spiking FeNeuron showed in section 5.2. The logical gates are in turn used to construct flip-flop circuits and the flip-flop circuits are used to construct counters, shift-registers and adders. The logical gates, therefore, are used as the basic building blocks for all of the digital circuits and their purpose is to control the movement of binary data and instructions.

5.3.1 Design of the clock

All digital systems use a master timing signal called clock. This two state timing signal is usually generated from an analog source and may be digitally tuned to meet frequency and phase requirements. For the Spiking FeNeuron CPU, the clock was generated from an adapted XOR ring oscillator. A very simplified version of this oscillator is presented as the first stage of the frequency divider in 5. Here, the input A is tied to logic 1 thereby creating an inverter. The output of the inverter is then feedback to input B. The frequency of the oscillator will depend

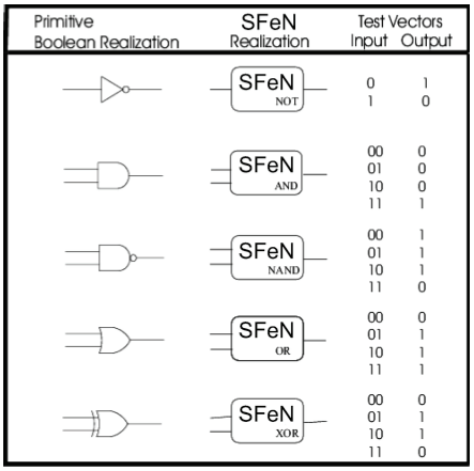


Fig. 7. The Spiking FeNeuron (SFeN) logical gates symbols and the test vectors after training.

on the delay of the feedback signal from the input to the output. Additional adapted XOR gates can be connected in scries to this one to some higher odd number to obtain the desired frequency of operation. As an observant reader may have noticed, a Spiking FeNeuron NOT gate could have been used in place of the Spiking FeNeuron XOR gate to derive the same results. The choice of the Spiking FeNeuron XOR gate does not provide any additional benefits over Spiking FeNeuron NOT gate but goes further to demonstrate the exibility of the Spiking FeNeuron logic. In standard CMOS logic, the NOT gate is almost always the only choice of a logic component for a ring oscillator due to its few transistor count of two. Compared to the 16-transistor count for a typical CMOS XOR gate, the area and ultimately cost savings in silicon makes the CMOS NOT gate the prime choice. In Spiking FeNeuron logic, however, each of the gates is derived from a single neuron trained to perform its function, thereby allowing tremendous area savings in hardware.

5.3.2 Design of the frequency divider circuit

A multi-stage frequency divider circuit can be implemented using addition and Spiking FeNeuron XOR gates. This circuit takes a clock as an input and provides three outputs with frequencies that are a divide by 2, by 4, and by 8 of the frequency of the input signal. The design schematic is presented together with the output waveform in Figure 8. On the schematic, CLK is the input clock signal, Y2 is the divide-by-2 output, Y3 is the divide-by-4 output, and Y4 is the divide-by-8 output.After training all of the gates, a function called Spiking FeNeuron was created which has two inputs: data vector and the option to select the desired logical gate required to perform a desired function. The output is the result from the selected gate.

5.3.3 Design of the D-type flip-flop

The D-type flip-flop is basically a SET-RESET latch with a small circuit modification. On the rising edge of the clock, the D input is latched to the output Q. The Spiking FeNeuron flip-flop logic circuit is shown in Figure 9. A test vector was generated to test the flip-flop in the example 1.

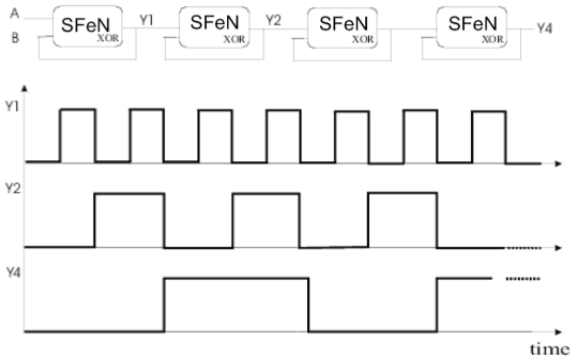


Fig. 8. The block diagram of the frequency divider with waveform.

MATLAB FUNCTION
function output = dff(data,clk)
data - input vector
clk - vector
output - response vector
EXAMPLE 1:
x = [0 0 1 1 1 0 1 0 1]
clk = [0 1 0 1 0 1 0 1 0]
output = dff(x,clk)
output = [0 0 0 1 0 0 0 0 0]

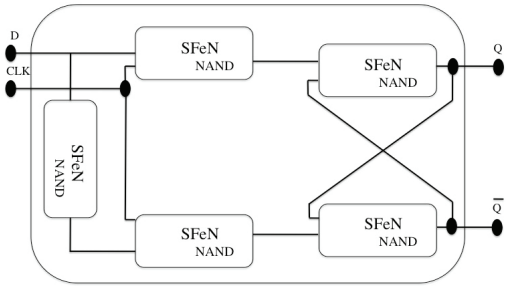


Fig. 9. The block diagram of D-flip-flop.

5.3.4 Design of the shift-register

A shift register is constructed using the flip-flop as shown in Figure 10. The shift register is a storage register that will move or shift the bits of the stored word either to the left or the right. The simulation of the Serial-In, Serial-Out (SISO) shift register is shown in example 3 with a test vector. The test vector with a 4-bit word [0110] is being applied to the shift registers input. The initial state of the shift register flip-flop output is 0. After the first clock pulse, the data stored is shifted one position to the right and the first bit of the applied serial word is shifted to the first position of the shifter register. After four clock pulses all the input data will be stored in the shift register. The summary of the test vector is shown in example 2.

MATLAB FUNCTION
function output = shiftreg(data)
data - input vector
clk - vector of the clock is generated inside the code
output - response vector
EXAMPLE 2:
output = shiftreg([1 0 0 1])
output = [0 0 0 0 1 0 0 0]

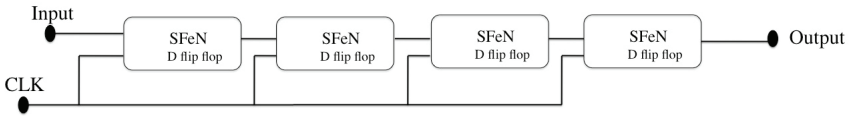


Fig. 10. The block diagram of the shift-register.

5.3.5 Design of the ALU

The ALU was construct using half-adder and full-adder circuits. The half-adder circuits were constructed using Spiking FeNeuron XOR and AND logic gates. The design schematic is presented on the right side of the Figure 11 where nodes A and B are the half-adder inputs, and S and carry denote the sum and the carry output signals respectively. The full-adder circuits were constructed from Spiking FeNeuron half-adders and Spiking FeNeuron logic gates. The design schematic is shown on the left side of the Figure 11 where A, B and CI represent the input and carry-in signals respectively. S and carry are the sum and carry outputs respectively. The full-adder was simulated for proper functionality. The results of this simulation are presented in example 3.
MATLAB FUNCTION
function [s,carryout] = fadder(data1,data2,carryin)
data1 - input vector
data2 - input vector
carryin - input of the carry
s - response vector of the sum
carryout - carry output

EXAMPLE 3:
data1 = [1 0 0 1]
data2 = [1 1 1 1]
$[s, c] = fadder(data1, data2, 0)$
s = [1 0 0 0]
c = 1

5.3.6 Design of a simple neural CPU

The Central Processing Unit contains an arithmetic-logic unit (ALU), a con- trol unit, and the registers for storage and manipulation of the data. The design of the CPU contains the ALU, a 32-bit 8x8 memory designed from Spiking FeNeuron D flip-flops. The system configuration of the CPU is shown on Figure 12. Information on the system bus which comprise CPU, memory control and data bhts was simulated with the use of switches. The binary instructions include memory and register access commands as well as ALU operational commands. The

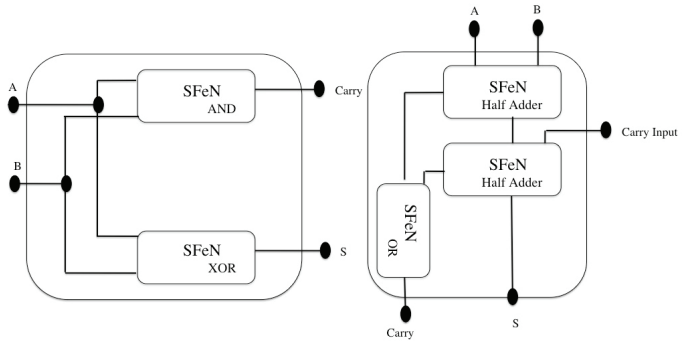


Fig. 11. The block diagram of the full adder.

microcode structure is shown on Table 2.
An example of some results for the instructions given to the CPU with 8 bits data is shown (Guerreiro et al., 2008).

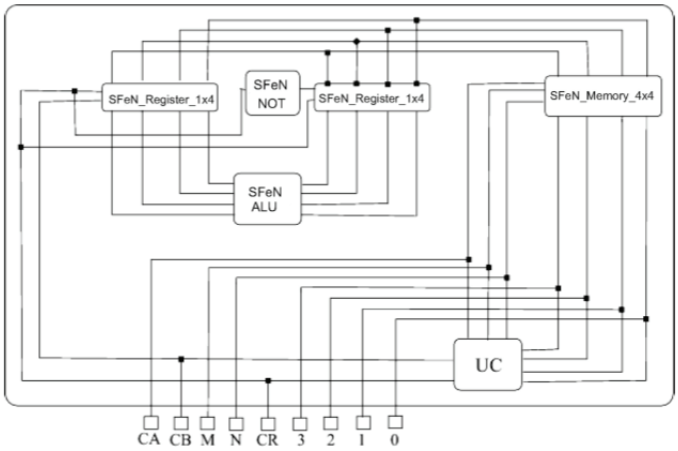


Fig. 12. The block diagram of the neural CPU.

Parameters	Name
CA	R/W operation memory
CB	R/W operation register
M and N	Memory Selector
CR	Register Selector
3/2/1/0	Data

Table 2. The microcode structure.

6. The Model of the FePerceptron in an FPGA

Now, this work is going to show the implementation of the FePerceptron model in a FPGA. For this implementation we are going to use the DSP builder tool of Altera Corporation. The DSP Builder technology allows you to go from system definition/simulation using the industry-standard the MathWorks/Simulink tools to the neuron implementation. The DSP Builder Signal Compiler block reads Simulink Model Files (.mdl) that are built using DSP Builder and MegaCoreÂő blocks and generates VHDL files and tool command language (Tcl) scripts for synthesis, hardware implementation, and simulation. The DSP builder automatically generate timing-optimized register transfer level (RTL) code based on high-level Simulink design descriptions (Altera, 2011).
In this way, first we developed the block diagram of the Simulink model of the FePerceptron which is shown in the Figure 13. The model is composed by the inputs, in this case two inputs as required by a Boolean logic gate, and the weights that were generated by the simulations in Matlab. After that the signal is summed and the output is generated passing the signal through the activation function that is implemented by the hystheresis of the FeCapacitor. The Figure 13 shows the implementation of the AND gate, for the other gates we only have to change the weights values, the same structure is used. The Table 3 shows the result of the simulations for the gates. Each gate is tested with the input vectors (Data1, Data2) and the output is seen by the display in Figure 13.

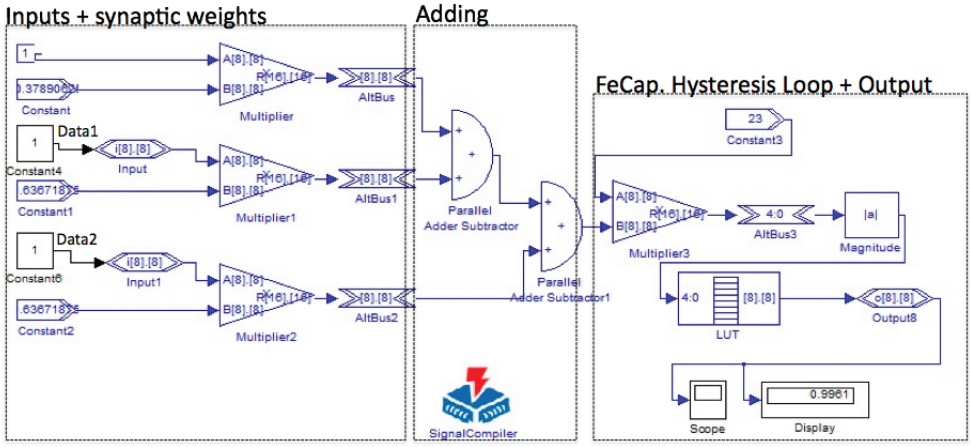


Fig. 13. The block diagram of the FePerceptron in Simulink (DSP Builder) for AND gate.

Data1	Data2	Display(AND)	Display(NAND)	Display(OR)	Display(NOR)
0	0	0	1	0	0.9961
0	1	0	0.9961	0.9973	0
1	0	0	0.9961	0.9973	0
1	1	0.9961	0	1	0

Table 3. The true table simulated by the simulink model of the FePerceptron.

The Simulink model then is converted to the RTL level code. Since the RTL level has a lot of details is not possible to show all in this work, more details can be found (VHDL, 2011).

7. Conclusion

The FeCapacitors have been embedded into LSIs as Ferroelectric Random Access Memory (FeRAM) and their reliability data have been accumulated for a long time. The capacitors are high impedance device, and it is an advantage for low power consumption, besides the configuration can be changed after packaging.

Thinking on this scenario, the FeCapacitor was choosen to be used in this work. It uses the phenomenon of the hysteresis loop of the FeCapacitor as the activation function for the artificial neuron models. We developed two models, the FePercetron and the FeSpiking Neuron Model, both models were first simulated in Matlab, and used to simulated the boolean functions. Since the FePerceptron were not able to simulated the XOR gate with a single neuron, because of the Perceptron characteristics. We were motivated to implement the FeSpiking that was based in the Extended Spiking Neuron Model and all logic gates were simulated, including the XOR. So, an adaptive simple CPU were developed, with simple logical circuits implemented, as registers, ALU, D-flip-flop as shown in section 4.

The FePerceptron and the FeSpiking Neuron Model presented the advantaged of being soft-programmable. This is accomplished by only adjusting the weight values of the synaptic connections without the need of changing all the architecture. It was firstly implemented by software verifying the success of the models.

From both models, first we chose the FePerceptron to be implemented in hardware because of the simplicity of the model. For this implementation we used the DSP builder tool of Altera Corporation. The DSP Builder Signal Compiler block read Simulink Model Files developed(.mdl) that were built using DSP Builder blocks and generated the VHDL files and the RTL level. This is the first step to develop more complex model as the FeSpiking Neuron Model, since the basic unit of the activation function (FeCapacitor) is already developed.

As hardware implementations, this model brings the contribution of being very simple, can save in silicon area, with low power consumption and being reconfigurable in two degrees of freedom, not only as characteristics intrinsic of the FPGA, but with the reconfigurability of the boolean gates. It is only necessary to change the values of the weights and the output is going to change to be the desired gate.

8. References

Altera Corporation. Diponível em: www.altera.com/products/dsp/dsp-builder.html. Acessado em: 10 de fevereiro de 2011.

Beiu, V.; Quintana, J. M.; Avendillo, M. J. (2003). *VLSI Implementations of Threshold Logic - A Comprehensive Survey*, Vol. 14, pp. 1217-1243.

Bermak, D.; Martinez, D. *A compact 3-D VLSI classifier using bagging threshold network ensembles* IEEE Transactions on Neural Networks 14(5) (2003) 1097âĂŞ1109.

Brown, B.; Yu, X.; Garverick, S. *A Mixed-mode analog VLSI continuous-time recurrent neural network* Proceedings of International Conference on Circuits, Signals and Systems, 2004,pp.104âĂŞ108.

Chen, Z.; Haykin, S; Becker, S. *Theory of monte carlo sampling-based alopex algorithms for neural networks*. Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing, pp. 17-21.

Dias, Fernando Morgado; Antunes, Ana; Manuel Mota, Alexandre. *Artificial neural networks: a review of commercial hardware* Engineering Applications of Artificial Intelligence, v.17 n.8, p.945-952, December, 2004

Duong, T.A. *Cascade error projection: an efficient hardware learning algorithm* Proceedings of the IEEE International Conference on Neural Networks, vol. 1, Perth, Australia, 1995, pp. 175-178.

Duong, T.A.; Stubberud, A.R., Convergence analysis of cascade error projection: an efficient hardware learning algorithm. International Journal of Neural System. v10 i3. 199-210.

D'Acierno, A. *Back-propagation learning algorithm and parallel computers: the CLEPSYDRA mapping scheme*. Neurocomputing. v31. 67-85.

Fakhraie, S.M.; Farshbaf, H; Smith, K.C. *Scalable closed-boundary analog neural networks*. IEEE Transactions on Neural Networks. v15. 492-504.

Glesner, M.; Poechmueller, W. *Neurocomputers: An Overview of Neural Networks in VLSI*. 1994. Chapman and Hall, London.

Guerreiro, Ana Maria GuimarÃčes; McMillan, Larry; Araujo, Carlos A Paz de. *Adaptive Logic Synthesis by Ferroelectric Spiking Neuron Circuits*. Integrated Ferroelectrics, v. 100, p. 238-253, 2008.

Haykin, S. (1998). *Neural Networks: A Comprehensive Foundation*. Prentice Hall, 2nd Edition.

Heemskerk, J. *Overview of neural hardware* Neurocomputers for Brain-Style Processing, Design, Implementation and Application, 1995.

Kumar, V.; Shekhar, S.; Amin, M. B. *A Scalable Parallel Formulation of the Backpropagation Algorithm for Hypercubes and Related Architectures* IEEE Transactions on Parallel and Distributed Systems, v.5 n.10, p.1073-1090, October 1994.

Ienne, Paolo; Cornu, Thierry; Kuhn, Gary. *Special-purpose digital hardware for neural networks: an architectural survey* Journal of VLSI Signal Processing Systems, v.13 n.1, p.5-25, Aug. 1996.

Jabri, Marwan; Flower, Barry. *Weight perturbation: An optimal architecture and learning technique for analog vlsi feedforward and recurrent multilayer networks.* Neural Computation, v.3 n.4, p.546-565, Winter 1991.

Janardan, Misra; Indranil, Saha. *Artificial neural networks in hardware: A survey of two decades of progress*. Journal Neurocomput. vol 74. 2010. ISSN: 0925-2312. Elsevier Science Publishers B. V.

Kung, S.Y. *Digital Neural Networks* Prentice-Hall, Upper Saddle River, NJ, USA, 1992.

Lehmann, Torsten; Bruun, Erik; Dietrich, Casper. *Mixed analog/digital matrix-vector multiplier for neural network synapses* Analog Integrated Circuits and Signal Processing, v.9 n.1, p.55-63, Jan. 1996.

Lamela, H.; and Ruiz-Llata, M. *Optoelectronic neural processor for smart vision applications*. Imaging Science Journal. v55 i4. 197-205.

Lenne, P. *Digital hardware architectures for neural networks* Speedup Journal 9(1)(1995)18âĂŞ25.

McCulloch, W. S.; Pitts, W. (1943). *A logical calculus of the ideas immanent in nervous activity*, Bull. Math. Biophysiol., vol. 5, pp. 115-133.

Mead, C. *Analog VLSI and Neural Systems* Addison-Wesley,Boston,MA, USA, 1989.

Miller, S. L.; Schwank, J. R.; Nasby, R. D.; and Rodgers, M. S. (1991). *Modeling Ferroelectric capacitor switching with asymmetric nonperiodic input signals and arbitrary initial conditions*. J. Appl. Phys., vol. 70, no. 5, pp. 2949-2860.

Moerland, P.D.; Fiesler, E; and Saxena, I. *Incorporation of liquid-crystal light valve nonlinearities in optical multilayer neural networks*. Applied Optics. v35. 5301-5307.

Nedjah, Nadia; Mourelle, Luiza de Macedo. *Reconfigurable hardware for neural networks: binary versus stochastic* Neural Computing and Applications, v.16 n.3, p.249-255, May 2007.

Patnaik, L.M.; Rao, R.N. *Parallel implementation of neocognitron on star topology: theoretical and experimental evaluation*. Neurocomputing. v41. 109-124.

RÃąk, ÃĄdÃąm; SoÃşs, BalÃązs Gergely; Cserey, GyÃűrgy. *Stochastic bitstream-based CNN and its implementation on FPGA* International Journal of Circuit Theory and Applications, v.37 n.4, p.587-612, May 2009.

Rosemblatt, F. (1958). *The perceptron: A probabilistic model for information storage and organization in the brain*. Psych. Revue, vol. 65, pp. 386-408.

Sheikholeslami, A.; Gulak, P. Glenn (1997). *A Survey of Behavioral Modeling of Ferroelectric Capacitors*. IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control vol. 44, no. 4, pp. 917-923.

Schmid, A.; Leblebici, Y.; and Mlynek, D. *A mixed analog digital artificial neural network with on chip learning*. IEE Proceedings-Circuits, Devices and Systems. 2004. v146. 345

Schrauwen, B.; D'Haene, M. *Compact digital hardware implementations of spiking neural networks* J. Van Campenhout (Ed.), Sixth FirW Ph.D. Symposium, 2005, in CD.

Shibata, T.; Ohmi, T. (1991). *An intelligent MOS transistor featuring gate-level weighted sum and threshold operations.* Technical Digest of International Electron Devices Meeting, Washigton DC, pp. 919-922.

Smieja, F. J. *Neural network constructive algorithms: trading generalization for learning efficiency* Circuits, Systems, and Signal Processing, v.12 n.2, p.331-374, 1993.

Sundararajan, N.; Saratchandran, P. *Parallel Architectures for Artificial Neural Networks: Paradigms and Implementations* IEEE Computer Society Press, Los Alamitos, CA, 1998.

Strey, Alfred; Avellana, Narcis. *A New Concept for Parallel Neurocomputer Architectures* Proceedings of the Second International Euro-Par Conference on Parallel Processing-Volume II, p.470-477, August 26-29, 1996.

Tokes, S.; OrzÃš, L.; Vr, G.; Roska, T. *Bacteriorhodopsin as an analog holographic memory for joint fourier implementation of CNN computers* Technical Report DNS-3-2000, Computer and Automation Research Institute of the Hungarian Academy of Sciences, Budapest, Hungary, 2000.

Valle, M. *Smart Adaptive Systems on Silicon*. 2005. Springer, Dordrecht, The Netherlands.

Verleysen, Michel; Thissen, Philippe; Voz, Jean-Luc; Madrenas, Jordi. *An Analog Processor Architecture for a Neural Network Classifier*, IEEE Micro, v.14 n.3, p.16-28, June 1994.

VHDL. Diponível em: ftp://alan:web@users.dca.ufrn.br. Acessado em: 20 de fevereiro de 2011.

Zhu, J.; Sutton, P. *FPGA implementations of neural networks-a survey of a decade of progress*. Field-Programmable Logic and Applications, vol. 2778. pp. 1062-1066.

Yang, F.; Paindavoine, M. *Implementation of an RBF neural network on embedded systems: real-time face tracking and identity verification*. IEEE Transaction on Neural Networks. v14 i5. 1162-1175.